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TOSHIBA

SERVICE MANUAL

COLOUR TELEVISION

28H37GZ

AK52 Chassis

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SM52-DRX_IF

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1.INTRODUCTION

11AK52 is a 100Hz flicker free colour television capable of driving 28”4:3/16:9, 32” 16:9, 33”4:3 and 29”4:3 real flat picture tubes.
The chassis is capable of operation in PAL, SECAM, NTSC (playback) colour standards and multiple transmission standards as B/G, D/K, I/I’, and L/L´.
Sound system output is supplying 2x10W (10%THD) for left and right outputs of 8ohm speakers.
TV supports the level 1.5 teletext standard. It is possible to decode transmissions including high graphical data.
The chassis is equipped with two full EuroScarts, one SCART for AV input/output, one front-AV input, one back-AV input, one headphone output, one SVHS input (via SCART and SVHS connector), two external speaker outputs (left and right).

2.TUNER

The hardware and software of the TV is suitable for tuners, supplied by different companies, which are selected from the Service Menu. These tuners can be combined VHF, UHF tuners suitable for CCIR systems B/G, H, L, L´, I/I´, and D/K. The tuning is available through the digitally controlled I^2C bus (PLL). Below you will find info on one of the Tuners in use.

General description of UV1316:
The UV1316 tuner belongs to the UV 1300 family of tuners, which are designed to meet a wide range of applications. It is a combined VHF, UHF tuner suitable for CCIR systems B/G, H, L, L’, I and I’. The low IF output impedance has been designed for direct drive of a wide variety of SAW filters with sufficient suppression of triple transient.

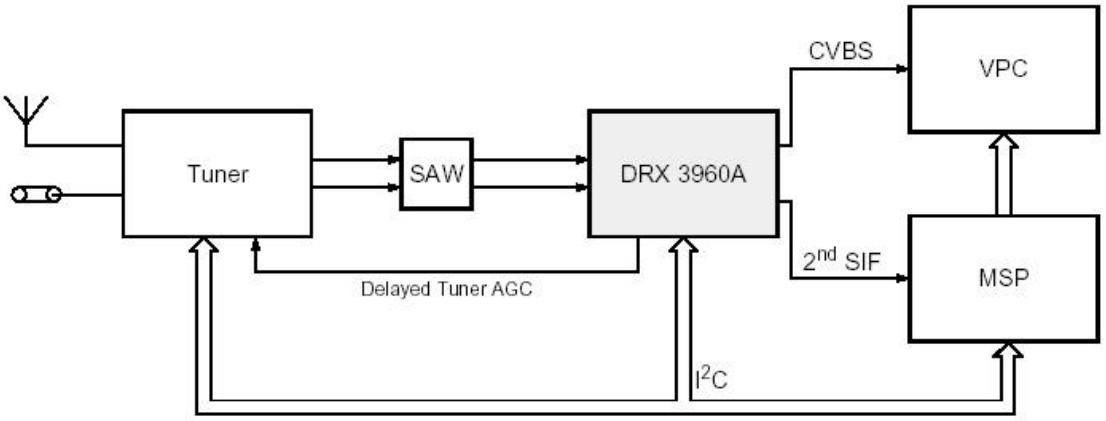
Features of UV1316:
1. Member of the UV1300 family small sized UHF/VHF tuners
2. Systems CCIR: B/G, H, L, L’, I and I’; OIRT: D/K
3. Digitally controlled (PLL) tuning via I^2C-bus
4. Off-air channels, S-cable channels and Hyperband
5. World standardized mechanical dimensions and world standard pinning
6. Compact size
7. Complies to “CENELEC EN55020” and “EN55013”

Pinning:

1.	Gain control voltage (AGC)	:	4.0V, Max: 4.5V
2.	Tuning voltage		
3.	I²C-bus address select	:	Max: 5.5V
4.	I²C-bus serial clock	:	Min:-0.3V, Max: 5.5V
5.	I²C-bus serial data	:	Min:-0.3V, Max: 5.5V
6.	Not connected		
7.	PLL supply voltage	:	5.0V, Min: 4.75V, Max: 5.5V
8.	ADC input		
9.	Tuner supply voltage	:	33V, Min: 30V, Max: 35V
10.	Symmetrical IF output 1		
11.	Symmetrical IF output 2		

3.IF PART (DRX 3960A)

Tuner output IF signal is pre-filtered with only one 8-MHz channel SAW filter. The entire multistandard processing is performed. The Digital Receiver Front-end DRX 3960A performs the entire multi-standard Quasi Split Sound (QSS) TV IF processing, AGC, video demodulation, and generation of the second sound IF (SIF). Video and tuner AGC is controlled and adjusted by take over voltage. The alignment-free DRX 3960A needs no special external components. All control functions and status registers are accessible via I^2C bus interface.



4.VIDEO SWITCH TEA6415

In case of three or more external sources are used, the video switch IC TEA6415 is used. The main function of this device is to switch 8 video-input sources on the 6 outputs.
Each output can be switched on only one of each input. On each input an alignment of the lowest level of the signal is made (bottom of sync. top for CVBS or black level for RGB signals).
Each nominal gain between any input and output is 6.5dB.For D2MAC or Chroma signal the alignment is switched off by forcing, with an external resistor bridge, 5VDC on the input. Each input can be used as a normal input or as a MAC or Chroma input (with external Resistor Bridge). All the switching possibilities are changed through the BUS. Driving 75ohm load needs an external resistor. It is possible to have the same input connected to several outputs.

5.MULTI STANDARD SOUND PROCESSOR

The MSP34x1G family of single-chip Multi-standard Sound Processors covers the sound processing of all analog TV-Standards worldwide, as well as the NICAM digital sound standards. The full TV sound processing, starting with analog sound IF signal-in, down to processed analog AF-out, is performed on a single chip. Signal conforming to the standard by the Broadcast Television Systems Committee (BTSC).
The DBX noise reduction, or alternatively, MICRONAS Noise Reduction (MNR) is performed alignment free. Other processed standards are the Japanese FM-FM multiplex standard (EIA-J) and the FM Stereo Radio standard.

6.SOUND OUTPUT STAGE WITH TDA7480L

The TDA7480L is an audio class-D amplifier assembled in Power DIP package specially designed for high efficiency applications mainly for TV and Home Stereo sets.
Mute stand-by function of the audio amplifier can be described as the following; the pin 12 (MUTE/STAND-BY) controls the amplifier status by two different thresholds, referred to ground. When Vpin 12 voltage is lower than 0.7V the amplifier is in Stand-by mode and the final stage generators are off. When Vpin 12 is higher than 4V, the amplifier is in play mode.
The TDA7480L is a 10W+10W stereo sound amplifier with mute/stand-by facility. MUTE control signal coming from microcontroller (when it is at high level) activates the mute function. IC is muted when mute pin is at low level (pin12). MUTE pin can also be activated via an external pop-noise circuitry in order to eliminate pop noise when TV is turned off. Just after the TV is turned off, this circuit switches the IC to stand-by mode by pulling the mute pin voltage to ground.

7.VERTICAL OUTPUT STAGE WITH TDA8177F

The IC TDA8177F is the vertical deflection booster circuit. Two supply voltages, +12V and -12V are needed to scan the inputs VERT+ and VERT-, respectively. And a third supply voltage, +60V for the flyback limiting are needed. The vertical deflection coil is connected in series between the output and feedback to the input.

8.VIDEO OUTPUT AMPLIFIER TDA6109

The TDA6109 includes three video output amplifiers in order to drive the three cathodes of a colour picture tube directly. To obtain maximum performance, the amplifier is used with black-current control.

9.POWER SUPPLY (SMPS)

The DC voltages required at various parts of the chassis are provided by an SMPS transformer controlled by the IC MC44608, which is designed for driving, controlling and protecting switching transistor of SMPS. The transformer generates 135V for FBT input, +/-14V for audio amplifier, 8V stand by voltage and 8V, 12V and 5V supplies for other different parts of the chassis.

An optocoupler is used to control the regulation of line voltage and stand-by power consumption. There is a regulation circuit in secondary side. This circuit produces a control voltage according to the changes in 135V DC voltage, via an optocoupler (TCET 1102G) to pin3 of the IC.

During the switch on period of the transistor, energy is stored in the transformer. During the switch off period energy is fed to the load via secondary winding. By varying switch-on time of the power transistor, it controls each portion of energy transferred to the second side such that the output voltage remains nearly independent of load variations.

10.MICROCONTROLLER SDA5550

10.1.General Features

• Feature selection via special function register
• Simultaneous reception of TTX, VPS, PDC, and WSS (line 23)
• Supply Voltage 2.5 and 3.3 V
• ROM version is used.

10.2.External Crystal and Programmable Clock Speed

• Single external 6MHz crystal, all necessary clocks are generated internally
• CPU clock speed selectable via special function registers.
• Normal Mode 33.33 MHz CPU clock, Power Save mode 8.33 MHz

10.3.Microcontroller Features

• 8bit 8051 instruction set compatible CPU.
• 33.33-MHz internal clock (max.)
• 0.360 ms (min.) instruction cycle
• Two 16-bit timers
• Watchdog timer
• Capture compare timer for infrared remote control decoding
• Pulse width modulation unit (2 channels 14 bit, 6 channels 8 bit)
• ADC (4 channels, 8 bit)
• UART (rxd, txd)

10.4.Memory

• Up to 128 Kilobyte on Chip Program ROM
• Eight 16-bit data pointer registers (DPTR)
• 256-bytes on-chip Processor Internal RAM (IRAM)
• 128bytes extended stack memory.
• Display RAM and TXT/VPS/PDC/WSS-Acquisition-Buffer directly accessible via MOVX
• UP to 16KByte on Chip Extended RAM (XRAM) consisting of;
- 1 Kilobyte on-chip ACQ-buffer-RAM (access via MOVX)
- 1 Kilobyte on-chip extended-RAM (XRAM, access via MOVX) for user software
- 3 Kilobyte Display Memory

10.5.Display Features

• ROM Character set supports all East and West European Languages in single device
• Mosaic Graphic Character Set
• Parallel Display Attributes
• Single/Double Width/Height of Characters
• Variable Flash Rate
• Programmable Screen Size (25 Rows x 33...64 Columns)
• Flexible Character Matrixes (HxV) 12 x 9...16
• Up to 256 Dynamical Redefinable Characters in standard mode; 1024 Dynamical Redefinable Characters in Enhanced Mode
• CLUT with up to 4096 colour combinations
• Up to 16 Colours per DRCS Character
• One out of 8 Colours for Foreground and Background Colours for 1-bit DRCS and ROM Characters

10.6.ROM Characters

• Shadowing
• Contrast Reduction
• Pixel by Pixel Shiftable Cursor With up to 4 Different Colours
• Support of Progressive Scan and 100 Hz.

• 3 X 4Bits RGB-DACs On-Chip
• Free Programmable Pixel Clock from 10 MHz to 32MHz
• Pixel Clock Independent from CPU Clock
• Multinorm H/V-Display Synchronization in Master or Slave Mode

10.7.Acquisition Features

• Multi-standard Digital Data Slicer
• Parallel Multi-norm Slicing (TTX, VPS, WSS, CC, G+)
• Four Different Framing Codes Available
• Data Caption only limited by available Memory
• Programmable VBI-buffer
• Full Channel Data Slicing Supported
• Fully Digital Signal Processing
• Noise Measurement and Controlled Noise Compensation
• Attenuation Measurement and Compensation
• Group Delay Measurement and Compensation
• Exact Decoding of Echo Disturbed Signals

10.8.Ports

• One 8-bit I/O-port with open drain output and optional I^2C Bus emulation support (Port0)
• Two 8-bit multifunction I/O-ports (Port1, Port3)
• One 4-bit port working as digital or analogue inputs for the ADC (Port2)
• One 2-bit I/O port with secondary function (P4.2, 4.3, 4.7)
• One 4-bit I/O-port with secondary function (P4.0, 4.1, 4.4) (Not available in P-SDIP 52)

11.SERIAL ACCESS 32K EEPROM

24LC32 is the 32Kbit electrically erasable programmable memory. The memory is compatible with the I^2C standard, two wire serial interface, which uses a bi-directional data bus and serial clock.

12.CLASS AB STEREO HEADPHONE DRIVER TDA1308

The TDA1308 is an integrated class AB stereo headphone driver contained in a DIP8 plastic package. The device is fabricated in a 1 mm CMOS process and has been primarily developed for portable digital audio applications.

13.SAW FILTERS

X6966M is an 8-MHz SAW Filter which is used for pre-filtering the IF input signal of DRX 3960A. The entire multistandard processing is performed within this filter which limits the signal bandwidth to 8 MHz and suppresses major parts of the adjacent channels.

14.IC DESCRIPTIONS

TDA6109
27W401
24LC32
SDA5275
DRAM 4MX4
SDA9400
LM317T
DDP3310
SDA5550
TEA6415
VPC3230D
TDA1308T
MSP3411G
TL431
DRX3960A
LM7808
BDX53BFI
TDA8177F
LM1086
MC44608
TCET1102G
TDA7480L
SAA3010T

14.1.TDA6109

14.1.1.General Description

The TDA6109JF includes three video output amplifiers in one plastic DIL-bent-SIL 9-pin medium power (DBS9MPF) package (SOT111-1), using high-voltage DMOS technology, and is intended to drive the three cathodes of a colour CRT directly. To obtain maximum performance, the amplifier should be used with black-current control.

14.1.2.Features

· Typical bandwidth of 9.0 MHz for an output signal of 60 V (p-p)
· High slew rate of 1850 V/ms
· No external components required
· Very simple application
· Single supply voltage of 200 V
· Internal reference voltage of 2.5 V
· Fixed gain of 51
· Black-Current Stabilization (BCS) circuit
· Thermal protection.

14.1.3.Pinning

SYMBOL	PIN	DESCRIPTION
$V_{i(1)}$	1	inverting input 1
$V_{i(2)}$	2	inverting input 2
$V_{i(3)}$	3	inverting input 3
GND	4	ground (fin)
I_{om}	5	black current measurement output
V_{DD}	6	supply voltage
$V_{oc(3)}$	7	cathode output 3
$V_{oc(2)}$	8	cathode output 2
$V_{oc(1)}$	9	cathode output 1

14.2.27W401

14.2.1.Description

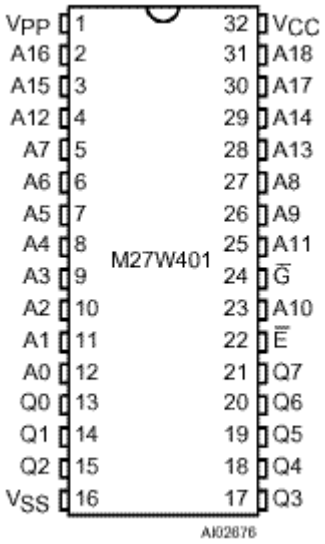
The M27W401 is a low voltage 4 Mbit EPROM offered in the two ranges UV (ultra violet erase) and OTP (one time programmable). It is ideally suited for microprocessor systems requiring large data or program storage and is organized as 524,288 by 8 bits. The M27W401 operates in the read mode with a supply voltage as low as 2.7V at –40 to 8??C temperature range. The decrease in operating power allows either a reduction of the size of the battery or an increase in the time between battery re-charges.
The FDIP32W (window ceramic frit-seal package) has a transparent lid, which allows the user to ex-pose the chip to ultraviolet light to erase the bit pat-tern. A new pattern can then be written to the device by following the programming procedure. For application where the content is programmed only one time and erasure is not required, the M27W401 is offered in PDIP32, PLCC32 and TSOP32 (8 x 20 mm) packages.

14.2.2.Features

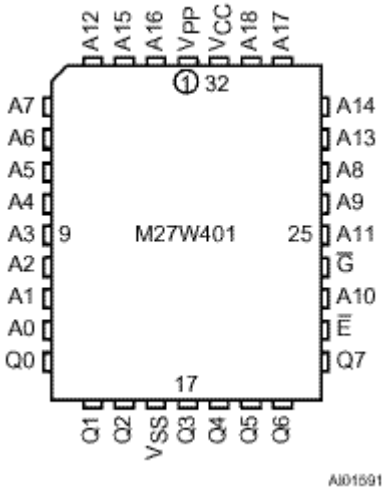
2.7V to 3.6v Low voltage in Read Operation
Access time:
–70ns at V_{CC} = 3.0V to 3.6V
–80ns at V_{CC} = 2.7V to 3.6V
Pin Compatible with M27C4001
Low Power Consumption:
–1?mA max Standby Current
– 15mA max Active Current at 5MHz
Programming Time 10?ns/byte
High Reliability CMOS Technology
– 2,000V ESD Protection
– 200mA Latchup Protection Immunity

Electronic Signature
– Manufacturer Code: 20h
– Device Code: 41h

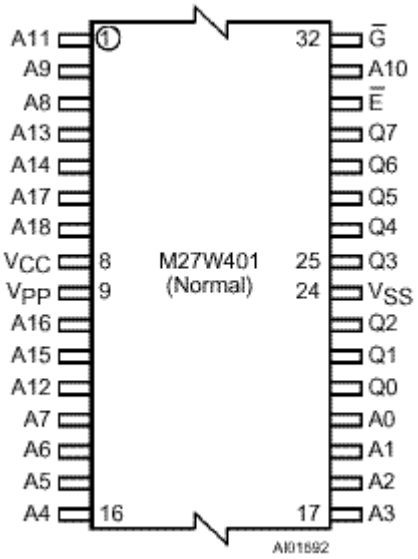
14.2.3.Connections



DIP connections



LCC Connections



TSOP Connections

Signal Names

A0-A18	Address Inputs
Q0-Q7	Data Outputs
E	Chip Enable
G	Output Enable
V_{pp}	Program Supply
V_{cc}	Supply Voltage
V_{ss}	Ground

14.3.24LC32A

14.3.1.Description

The Microchip Technology Inc. 24LC32A is a 4K x 8 (32K bit) Serial Electrically Erasable PROM capable of operation across a broad voltage range (2.5V to 6.0V). It has been developed for advanced, low power applications such as personal communications or data acquisition. The 24LC32A also has a page-write capability of up to 32 bytes of data. The 24LC32A is capable of both random and sequential reads up to the 32K boundary. Functional address lines allow up to eight 24LC32A devices on the same bus, for up to 256K bits address space. Advanced CMOS technology and broad voltage range make this device ideal for low-power/ low-voltage, nonvolatile code and data applications. The 24LC32A is available in the standard 8-pin plastic DIP and both 150 mil and 200 mil SOIC packaging.

14.3.2.Features

• Single supply with operation down to 2.5V
• Maximum write current 3 mA at 6.0V
• Standby current 1 mA max at 2.5V
• 2-wire serial interface bus, I 2 CÔ compatible
• 100 kHz (2.5V) and 400 kHz (5V) compatibility
• Self-timed ERASE and WRITE cycles
• Power on/off data protection circuitry
• Hardware write protect
• 1,000,000 Erase/Write cycles guaranteed
• 32 byte page or byte write modes available

• Schmitt trigger filtered inputs for noise suppression
• Output slope control to eliminate ground bounce
• 2 ms typical write cycle time, byte or page
• Up to eight devices may be connected to the same bus for up to 256K bits total memory
• Electrostatic discharge protection > 4000V
• Data retention > 200 years
• 8-pin PDIP and SOIC packages
• Temperature ranges
• Commercial (C): 0°C to +75°C
• Industrial (I): -40°C to +85°C

14.3.3.Pin Descriptions

A0, A1, A2 Chip Address Inputs
The A0..A2 inputs are used by the 24LC32A for multiple device operation and conform to the 2-wire bus standard. The levels applied to these pins define the address block occupied by the device in the address map. A particular device is selected by transmitting the corresponding bits (A2, A1, A0) in the control byte.

SDA Serial Address/Data Input/Output
This is a Bi-directional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pull up resistor to VCC (typical 10 kO for 100 kHz, 2 kO for 400 kHz) For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL HIGH are reserved for indicating the START and STOP conditions.

SCL Serial Clock
This input is used to synchronize the data transfer from and to the device.
WP
This pin must be connected to either VSS or VCC. If tied to VSS, normal memory operation is enabled (read/write the entire memory 000-FFF). If tied to VCC, WRITE operations are inhibited. The entire memory will be write-protected. Read operations are not affected.
WCC
+2.5V to 6V Power Supply
WSS
Ground

14.4.SDA5275

14.4.1.Features

• Single chip teletext IC
• Analog CVBS-input with onchip clamping circuitry
• Slicer
• Supports level 1, 2.5 and 3.5 ETSI teletext standard
• Stores up to 14 teletext pages on chip
• Stores up to 2048 teletext pages with external 16 M memory
• SDA 5275: full level 2.5 processing
• Analog RGB-output
• 41 Latin script languages
• 12 ´ 10 character size
• Parallel display attributes
• 64 from 4096 colors selectable
• Enhanced flash modes
• Dynamically redefinable character set (DRCS, PCS)
• Pixel graphics
• Full screen display (64 ´ 32 or 80 ´ 24 character positions)
• Horizontal and vertical scrolling
• Graphic cursors
• 4:3 and 16:9 display
• Multinorm display (50/60/100/120 Hz)
• RISC-processor
• Firmware downloadable
• I^2C / 3 wire UART-interface (1 Mbit/s)
• Independent clocks for acquisition and display

• Tools for greatly simplified software development
• 24-Kbyte on-chip reconfigurable DRAM
• 44160-bit character ROM
• One external crystal for all standards

14.4.2.Pin Definition and functions

Pin No. P-LCC-68-1	Symbol	Function
1	INTQ	Interrupt request output to ext. controller
2	CLK-IO	System clock input/output
3	TCSQ/FLD	Composite sync output/ field output
4	VS/VCS	Vertical sync input/output
5	HS	Horizontal sync input/output
6	XOUT	20.5-MHz crystal oscillator output
7	XIN	20.5-MHz crystal oscillator input
8	GPO	General purpose output
9	TM	Test pin, leave open or connect VSS
10	CVBS	CVBS-video signal input
11	VDD1	+ 5 V digital supply
12	VDDA	+ 5 V analog supply
13	VSSA1	Analog ground
14	N.C.	Not connected
15	N.C.	Not connected
16	VDD2	+ 5 V digital supply
17	RES	Chip reset
18	N.C.	Not connected
19	N.C.	Not connected
20	N.C.	Not connected
21	VDD3	+ 5 V digital supply
22	N.C.	Not connected
23	VREF	+ 3 V reference voltage input
24	N.C.	Not connected
25	VDD4	+ 5 V digital supply
26	A8	External DRAM-address
27	A7	External DRAM-address
28	A6	External DRAM-address
29	A5	External DRAM-address
30	A4	External DRAM-address
31	A3	External DRAM-address
32	A2	External DRAM-address
33	A1	External DRAM-address
34	A0	External DRAM-address
35	A9	External DRAM-address
36	A10	External DRAM-address
37	A11	External DRAM-address
38	RASQ	Row address strobe (DRAM)
39	WEQ	Write enable (DRAM)
40	D1	External DRAM-data
41	D0	External DRAM-data
42	D2	External DRAM-data
43	D3	External DRAM-data
44	VSS4	0 V digital supply
45	CASQ	Column address strobe
46	N.C.	Not connected
47	N.C.	Not connected
48	N.C.	Not connected
49	VSS3	0 V digital supply
50	N.C.	Not connected
51	N.C.	Not connected
52	N.C.	Not connected
53	N.C.	Not connected
54	N.C.	Not connected
55	VSS2	0 V digital supply
56	VBB	Substrate bias voltage N.C.* (depends on version)
57	N.C.	Not connected

58	VSSA2	Analog ground
59	RGB-GND	RGB-ground
60	VSS1	0 V digital supply
61	R	Analog red display output
62	G	Analog green display output
63	B	Analog blue display output
64	BLAN	Blanking signal open drain output
65	CORQ	Contrast reduction open drain output
66	SCL	Bi-directional I^2C Bus clock port
67	SDA	Bi-directional I^2C Bus data port
68	I^2CEN	I^2C Bus enable

14.5.DRAM 4MX4

14.5.1.General Description

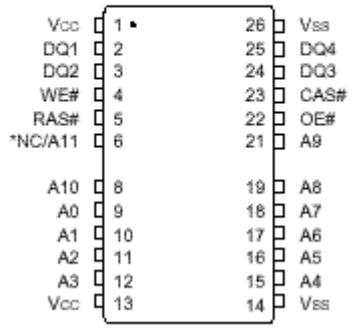
The 4 Meg x 4 DRAM is a randomly accessed, solid-state memory containing 16,777,216 bits organized in a x4 con-figuration. RAS# is used to latch the row address (first 11 bits for 2K and first 12 bits for 4K). Once the page has been opened by RAS#, CAS# is used to latch the column address (the latter 11 bits for 2K and the latter 10 bits for 4K, address pins A10 and A11 are “don’t care”). READ and WRITE cycles are selected with the WE# input. A logic HIGH on WE# dictates READ mode, while a logic LOW on WE# dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE# or CAS#, whichever occurs last. An EARLY WRITE occurs when WE# is taken LOW prior to CAS# falling. A LATE WRITE or READ-MODIFY-WRITE occurs when WE# falls after CAS# is taken LOW. During EARLY WRITE cycles, the data outputs (Q) will remain High-Z regardless of the state of OE#. During LATE WRITE or READ-MODIFY-WRITE cycles, OE# must be taken HIGH to disable the data outputs prior to applying input data. If a LATE WRITE or READ-MODIFY-WRITE is attempted while keeping OE# LOW, no write will occur, and the data outputs will drive read data from the accessed location. The four data inputs and the four data outputs are routed through four pins using common I/O, and pin direction is controlled by WE# and OE#.

14.5.2.Features

- Industry-standard x4 pin out, timing, functions and packages
- State-of-the-art, high-performance, low-power CMOS silicon-gate process
- Single power supply (+3.3V ±0.3V or +5V ±10%)
- All inputs, outputs and clocks are TTL-compatible
- Refresh modes: RAS#-ONLY, HIDDEN and CAS#-BEFORE - RAS# (CBR)
- Optional Self Refresh (S) for low-power data retention
- 11 row, 11 column addresses (2K refresh) or 12 row, 10 column addresses (4K refresh)
- Extended Data-Out (EDO) PAGE MODE access cycle
- 5V-tolerant inputs and I/Os on 3.3V devices

14.5.3.Pin Assignment

24/26-Pin SOJ
(DA-2)



Top View

*NC on 2K refresh and A11 on 4K refresh options. **Note:** The “#” symbol indicates signal is active LOW.

14.6.SDA9400

14.6.1.General Description

The SDA9400 is a new component of the Micronas MEGAVISION ® IC set in a 0.35µm embedded DRAM technology (frame memory embedded). The SDA9400 is pin compatible to the SDA9401 (field memory embedded). The SDA9400 comprises all main functionalities of a digital feature box in one monolithic IC. The scan rate conversion to 100/120 Hz interlaced (50/60 Hz progressive) is based on a motion adaptive algorithm. The scan rate converted picture can be vertically expanded. The SDA9400 has a free running mode, therefore features like scan rate conversion to e.g. 70, 75 Hz with joint lines or multiple picture display (e.g. tuner scan) are possible. Due to the frame based signal processing, the noise reduction has been greatly improved. Furthermore separate motion detectors for luminance and chrominance have been implemented. For automatic controlling of the noise reduction parameters a noise measurement algorithm is included, which measures the noise level in the picture or in the blanking period. In addition a spatial noise reduction is implemented, which reduces the noise even in the case of motion. The input signal can be compressed horizontally and vertically with a certain number of factors. Therefore split screen is supported. Beside these additional functions like coloured background, windowing and flashing are implemented.

14.6.2.Features

• Two input data formats
- 4:2:2 luminance and chrominance parallel (2 x 8 wires)
- ITU-R 656 data format (8 wires)

• Two different representations of input chrominance data
- 2's complement code
- Positive dual code

• Flexible input sync controller

• Flexible compression of the input signal
- Digital vertical compression of the input signal (1.0, 1.25, 1.5, 1.75, 2.0, 3.0, 4.0)
- Digital horizontal compression of the input signal (1.0, 2.0, 4.0)

• Noise reduction
- Motion adaptive spatial and temporal noise reduction (3D-NR)
- Temporal noise reduction for luminance frame based or field based
- Temporal noise reduction for chrominance field based
- Separate motion detectors for luminance and chrominance
- Flexible programming of the temporal noise reduction parameters
- Automatic measurement of the noise level (5-bit value, readable by I²C bus)

• 3-D motion detection
- High performance motion detector for scan rate conversion
- Global motion detection flag (readable by I²C bus)
- Movie mode and phase detector (readable by I²C bus)

• TV mode detection by counting line numbers (PAL, NTSC, readable by I²C bus)

• Embedded memory
- 5 Mbit embedded DRAM core for field memories
- 192 kbit embedded DRAM core for line memories

• Flexible clock and synchronization concept
- Decoupling of the input and output clock system possible

• Scan rate conversion
- Motion adaptive 100/120 Hz interlaced scan conversion
- Motion adaptive 50/60 Hz progressive scan conversion
- Simple static interlaced and progressive conversion modes for 100/120 Hz interlaced or 50/60 Hz progressive scan conversion: e.g. ABAB, AABB, AA*B*B, AAAA, BBBB, AB, AA*
- Simple progressive scan conversion with joint lines:
50 Hz -> 60, 70, 75 Hz progressive
60 Hz -> 70, 75 Hz progressive
- Large area and line flicker reduction

• Flexible digital vertical expansion of the output signal (1.0, ... [1/32] ..., 2.0)

• Flexible output sync controller
- Flexible positioning of the output signal
- Flexible programming of the output sync raster
- External synchronization by backend IC possible
(e.g. split screen for one TV channel with joint lines and one PC VGA channel)

• **Signal manipulations**
- Insertion of coloured background
- Vertical and/or horizontal windowing with four different speed factors
- Flash generation (for supervising applications, motion flag readable by I²C bus)
- Still frame or field
- Support of split screen applications
- Multiple picture display - Tuner scan (4 and 16 times for 4:3, 12 times for 16:9 tubes)
- Support of multi picture display with PIP or front-end processor with integrated scaler
(e.g. 9 times display of PIP pictures, picture tracking, random pictures, still-in-moving picture, moving-in-still picture)
• I²C-bus control (400 kHz)
• P-MQFP-64 package
• 3.3 V ± 5% supply voltage

14.6.3.Pin Definition

Pin No.	Name	Type	Description
2,8,24,42,55	VSS1	S	Supply voltage (*V* SS = 0 V)
9,25,41,56	VDD1	S	Supply voltage (*V* DD = 3.3 V)
36,52,58	VSS2	S	Supply voltage (*V* SS = 0 V)
35,51,53,57,59	VDD2	S	Supply voltage (*V* DD = 3.3 V)
43,..,50	YIN0...7	I/TTL	Data input Y (see input data format)
31,..,34;37,...,40	UVIN0...7	I/TTL PD	Data input UV (for 4:2:2 parallel, see input data format) (for CCIR 656, see input data format)
30	RESET	I/TTL	System reset. The RESET input is low active. In order to ensure correct operation a "Power On Reset" must be performed. The RESET pulse must have a minimum duration of two clock periods of the system clock CLK1.
23	HIN	I/TTL PD	H-Sync input (only for full CCIR 656)
22	VIN	I/TTL PD	V-Sync input (only for full CCIR 656)
29	SYNCEN	I/TTL	Synchronization enable input
21	SDA	I/O	I²C-Bus data line (5V ability)
20	SCL I	I	I²C-Bus clock line (5V ability)
54	CLK1	I/TTL	System clock 1
17,..,10	UVOUT0...7	O/TTL	Data output UV (see output data format)
7,..,3;1;64;63	YOUT0...7	O/TTL	Data output Y (see output data format)
62	HREF	O/TTL	Horizontal active video output
61	VOUT/ VEXT	I/O/ TTL	EXSYN=0 (I²C-bus parameter): V-Sync output EXSYN=1: External V-Sync input for output part
60	HOUT/ HEXT	I/O/ TTL	EXSYN=0 (I²C-bus parameter): H-Sync output EXSYN=1: External H-Sync input for output part
18	INTERLACED	O/TTL	Interlace signal for AC coupled vertical deflection
28	X1 / CLK2	I/TTL	Crystal connection / System clock 2
27	X2	O/AN	Crystal connection
26	CLKOUT	O/TTL	Clock output (depends on I²C parameters CLK11EN, CLK21EN, FREQR)
19	TEST	I/TTL	Test input, connect to *V* SS for normal operation

14.7.LM317T

14.7.1.Description

The LM317T is an adjustable 3 terminal positive voltage regulator capable of supplying in excess of 1.5 amps over an output range of 1.25 to 37 volts. This voltage regulator is exceptionally easy to use and requires only two external resistors to set the output voltage. Further, it employs internal current limiting, thermal shutdown and safe area compensation, making it essentially blow–out proof. The LM317 serves a wide variety of applications including local, on card regulation. This device can also be used to make a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM317 can be used as a precision current regulator.

14.7.2.Features

• Output Current in Excess of 1.5 A

• Output Adjustable between 1.2 V and 37 V
• Internal Thermal Overload Protection
• Internal Short Circuit Current Limiting Constant with Temperature
• Output Transistor Safe–Area Compensation
• Floating Operation for High Voltage Applications
• Available in Surface Mount D^2PAK, and Standard 3–Lead Transistor Package
• Eliminates Stocking many Fixed Voltages

14.8.DDP3310

14.8.1.Description

The DDP 3310B is a single-chip digital Display and Deflection Processor designed for high-quality back-end applications in 100/120-Hz TV sets with 4:3 or 16:9 picture tubes. The IC can be combined with members of the DIGIT 3000 IC family (VPC 32xx, TPU 3040), or it can be used with third-party products. The IC contains the entire digital video component and deflection processing and all analog interface components.

14.8.2.Features

Video processing

– linear horizontal scaling (0.25 … 4)
– non-linear horizontal scaling “panorama-vision”
– dynamic peaking
– soft limiter (gamma correction)
– color transient improvement
– programmable RGB matrix
– picture frame generator
– two analog RGB/Fast-Blank inputs. The DDP 3310B is a single-chip digital Display and Deflection Processor designed for high-quality back-

Deflection processing

– scan velocity modulation output
– high-performance H/V deflection
– EHT compensation for vertical / East/West
– soft start/stop of H-Drive
– vertical angle and bow
– differential vertical output
– vertical zoom via deflection
– horizontal and vertical protection circuit
– adjustable horizontal frequency for VGA/SVGA display

Miscellaneous

– selectable 4:1:1/ 4:2:2 YC $_r$ C $_b$ input
– selectable 27/ 32-MHz line-locked clock input
– crystal oscillator for horizontal protection
– automatic picture tube adjustment (cutoff, white-drive)
– single 5-V power supply
– hardware for simple 50/60-Hz to 100/ 120-Hz conversion (display frequency doubling)
– two I^2C-controlled PWM outputs
– beam current limiter

14.8.3.Pin connection and short descriptions

NC = not connected
X = obligatory; connect as described in circuit diagram
OUT = Output
LV = if not used, leave vacant
IN = Input
SUPPLY = Supply Pin

Pin no PLCCK 68 pin	Pin name	Type	Connection (if not used)	Short description
1	VSUPP	SUPPLY	X	Supply voltage, Output pin driver
2	GNDP	SUPPLY	X	Ground, Output pin driver
3	VS2	IN	GNDD	Additional VSYNC input
4	FIFORRD	OUT	LV	FIFO Read counter reset

5	FIFORD	OUT	LV	FIFO Read Enable
6	FIFOWR	OUT	LV	FIFO Write Enable
7	FIFORWR	OUT	LV	FIFO Write counter reset
8	HOUT	OUT	X	Horizontal Drive Output
9	HFLB	IN	Hout	Horizontal Flyback Input
10	SAFETY	IN	GNDO	Safety Input
11	VPROT	IN	GNDO	Vertical protection Input
12	FREQSEL	IN	X	Selection of H-Drive Frequency Range
13	CM1	IN	X	Clock select 40.5 or 27/32 MHz
14	CMO	IN	X	Clock select 27/32 MHz
15	RSW2	OUT	LV	Range Switch2, Measurement ADC
16	RSW1	IN/OUT	LV	Range Switch1, Measurement ADC
17	SENSE	IN	GNDO	Sense ADC Input
18	GNDM	SUPPLY	X	Ground, MADC Input
19	VERT+	OUT	GNDO	Differantial Vertical Sawtooth Output
20	VERT-	OUT	GNDO	Differantial Vertical Sawtooth Output
21	EW	OUT	GNDO	Vertical Parabola Output
22	XREF	IN	X	Reference Input for RGB DACs
23	SVM	OUT	VSUPO	Scan Velocity Modulation
24	ROUT	OUT	VSUPO	Analog Output Red
25	GOUT	OUT	VSUPO	Analog Output Green
26	BOUT	OUT	VSUPO	Analog Output Blue
27	GNDO	SUPPLY	X	Ground, Analog Back-end
28	VSUPO	SUPPLY	X	Supply Voltage, Analog Back-end
29	VRD/BCS	IN	X	DAC Reference, Beam Current Safety
30	FBLIN1	IN	GNDO	Fast-Blank1 Input
31	RIN1	IN	GNDO	Analog Red1 Input
32	GIN1	IN	GNDO	Analog Green1 Input
33	BIN1	IN	GNDO	Analog Blue1 Input
34	FBLIN2	IN	GNDO	Fast-Blank2 Input
35	RIN2	IN	GNDO	Analog Red2 Input
36	GIN2	IN	GNDO	Analog Green2 Input
37	BIN2	IN	GNDO	Analog Blue2 Input
38	TEST	IN	GNDD	Test Pin
39	RESQ	IN	X	Reset Input, active low
40	PWM1	OUT	LV	I^2C-controlled DAC
41	PWM2	OUT	LV	I^2C-controlled DAC
42	HCS	IN	GNDD	Half-contrast
43	C0	IN	GNDD	Picture Bas Chroma (LSB)
44	C1	IN	GNDD	Picture Bas Chroma
45	C2	IN	GNDD	Picture Bas Chroma
46	C3	IN	GNDD	Picture Bas Chroma
47	C4	IN	GNDD	Picture Bas Chroma
48	C5	IN	GNDD	Picture Bas Chroma
49	C6	IN	GNDD	Picture Bas Chroma
50	C7	IN	GNDD	Picture Bas Chroma (MSB)
51	VSUPD	SUPPLY	X	Supply Voltage, Digital Circuitry
52	GNDD	SUPPLY	X	Ground, Digital Circuitry
53	LLC2	IN	X	System Clock Input (27/32/40.5 MHz)
54	Y0	IN	GNDD	Picture Bas Luma (LSB)
55	Y1	IN	GNDD	Picture Bas Luma
56	Y2	IN	GNDD	Picture Bas Luma
57	Y3	IN	GNDD	Picture Bas Luma
58	Y4	IN	GNDD	Picture Bas Luma
59	Y5	IN	GNDD	Picture Bas Luma
60	Y6	IN	GNDD	Picture Bas Luma
61	Y7	IN	GNDD	Picture Bas Luma (MSB)
62	LLC1	IN	VSUPD	Single Line-Locked Clock Input (13.5/16 MHz)
63	HS	IN	X	Horizontal Sync Input
64	VS	IN	GNDD	Vertical Sync Input
65	XTALK2	OUT	X	Analog Crystal Output (5-MHz Security Clock)
66	XTALK1	IN	X	Analog Crystal Input (5-MHz Security Clock)
67	SDA	IN/OUT	X	I^2C-Bus Data
68	SCL	IN/OUT	X	I^2C-Bus Clock

14.9.SDA5550

14.9.1.General definition

The SDA5550M is a single chip teletext decoder for decoding World System Teletext data as well as Video Programming System (VPS), Program Delivery Control (PDC), and Wide Screen Signalling (WSS) data used for PAL plus transmissions (Line 23). The device provides an integrated general-purpose, fully 8051-compatible Microcontroller with television specific hardware features. Microcontroller has been enhanced to provide powerful features such as memory banking, data pointers, and additional interrupts etc. The on-chip display unit for displaying Level 1.5 teletext data can also be used for customer defined on screen displays. Internal XRAM consists of up to 17 Kbytes. This device can support external memory up to 1Mbyte ROM and RAM.TVTEXT Controller contains a data slicer for VPS, WSS, PDC and TXT, an acceleration acquisition hardware module, a display generator for Level 1.5 TXT and powerful On screen Display capabilities based on parallel attributes, and pixel oriented characters (DRCS). The 8 bit Microcontroller operates at 360nsec cycle time (min). Controller with dedicated hardware does most of the internal TXT acquisition processing, transfer data to/from external memory interface and receives/transmits data via I^2C-firmware user interface. SDA5550M is realized in 0.25 micron technology with 2.5V supply voltage and 3.3V I/O compatible. The IC produces the following input or output control signals; AGC_CON, MODE_SW, L / L', PIP_MODS, PIP_SEL, ON/OFF (stand-by), SC1..3_IN_AV (pin 8 information from 3 SCARTs), AFC, MUTE (to mute audio output IC), I^2CEN.

14.9.2.Features

General

- Feature selection via special function register
- Simultaneous reception of TTX, VPS, PDC, and WSS (line 23)
- Supply Voltage 2.5 and 3.3 V

External Crystal and Programmable clock speed

Single external 6MHz crystal, all necessary clocks are generated internally
CPU clock speed selectable via special function registers.
Normal Mode 33.33 MHz CPU clock, Power Save mode 8.33 MHz

Microcontroller Features

- 8bit 8051 instruction set compatible CPU.
- 33.33-MHz internal clock (max.)
- 0.360ms (min.) instruction cycle
- Two 16-bit timers
- Watchdog timer
- Capture compare timer for infrared remote control decoding
- Pulse width modulation unit (2 channels 14 bit, 6 channels 8 bit)
- ADC (4 channels, 8 bit)
- UART

Memory

- Non-multiplexed 8-bit data and 16 … 20-bit address bus (ROMless Version)
- Memory banking up to 1Mbyte (Romless version)
- Up to 128 Kilobyte on Chip Program ROM
- Eight 16-bit data pointer registers (DPTR)
- 256-bytes on-chip Processor Internal RAM (IRAM)
- 128bytes extended stack memory.
- Display RAM and TXT/VPS/PDC/WSS-Acquisition-Buffer directly accessible via MOVX
- UP to 16KByte on Chip Extended RAM (XRAM) consisting of;
- 1 Kilobyte on-chip ACQ-buffer-RAM (access via MOVX)
- 1 Kilobyte on-chip extended-RAM (XRAM, access via MOVX) for user software
- 3 Kilobyte Display Memory

Display Features

- ROM Character Set Supports all East and West European Languages in single device
- Mosaic Graphic Character Set
- Parallel Display Attributes
- Single/Double Width/Height of Characters

• Variable Flash Rate
• Programmable Screen Size (25 Rows x 33...64 Columns)
• Flexible Character Matrixes (HxV) 12 x 9...16
• Up to 256 Dynamical Redefinable Characters in standard mode; 1024 Dynamical Redefinable Characters in Enhanced Mode
• CLUT with up to 4096 color combinations
• Up to 16 Colors per DRCS Character
• One out of Eight Colors for Foreground and Background Colors for 1-bit DRCS and ROM Characters
• Shadowing
• Contrast Reduction
• Pixel by Pixel Shiftable Cursor With up to 4 Different Colors
• Support of Progressive Scan and 100 Hz.
• 3 X 4Bits RGB-DACs On-Chip
• Free Programmable Pixel Clock from 10 MHz to 32MHz
• Pixel Clock Independent from CPU Clock
• Multinorm H/V-Display Synchronization in Master or Slave Mode

Acquisition Features
• Multistandard Digital Data Slicer
• Parallel Multi-norm Slicing (TTX, VPS, WSS, CC, G+)
• Four Different Framing Codes Available
• Data Caption only Limited by available Memory
• Programmable VBI-buffer
• Full Channel Data Slicing Supported
• Fully Digital Signal Processing
• Noise Measurement and Controlled Noise Compensation
• Attenuation Measurement and Compensation
• Group Delay Measurement and Compensation
• Exact Decoding of Echo Disturbed Signals

Ports
• One 8-bit I/O-port with open drain output and optional I^2C Bus emulation support (Port 0)
• Two 8-bit multifunction I/O-ports (Port 1, Port 3)
• One 4-bit port working as digital or analog inputs for the ADC (Port 2)
• One 2-bit I/O port with secondary functions (P4.2, 4.3, 4.7)
• One 4-bit I/O-port with secondary function (P4.0, 4.1, 4.4) (Not available in P-SDIP 52)

14.10.TEA6415C

14.10.1.General Description

The main function of the IC is to switch 8 video input sources on 6 outputs. Each output can be switched on only one of each input. On each input an alignment of the lowest level of the signal is made (bottom of synch. top for CVBS or black level for RGB signals). Each nominal gain between any input and output is 6.5dB. For D2MAC or Chroma signal the alignment is switched off by forcing, with an external resistor bridge, 5 V_{DC} on the input. Each input can be used as a normal input or as a MAC or Chroma input (with external resistor bridge). All the switching possibilities are changed through the BUS. Driving 75? load needs an external transistor. It is possible to have the same input connected to several outputs. The starting configuration upon power on (power supply: 0 to 10V) is undetermined. In this case, 6 words of 16 bits are necessary to determine one configuration. In other case, 1 word of 16 bits is necessary to determine one configuration.

14.10.2.Features

• 20MHz Bandwidth
• Cascadable with another TEA6415C (Internal address can be changed by pin 7 voltage)
• 8 Inputs (CVBS, RGB, MAC, CHROMA,...)
• 6 Outputs
• Possibility of MAC or chroma signal for each input by switching-off the clamp with an external resistor bridge
• Bus controlled
• 6.5dB gain between any input and output
• 55dB crosstalk at 5mHz

• Fully ESD protected

14.10.3.Pinning

1.	Input	:	Max : 2Vpp, Input Current: 1mA, Max: 3mA
2.	Data	:	Low level : -0.3V Max: 1.5V, High level : 3.0V Max : Vcc+0.5V
3.	Input	:	Max : 2Vpp, Input Current: 1mA, Max : 3mA
4.	Clock	:	Low level : -0.3V Max: 1.5V, High level : 3.0V Max : Vcc+0.5V
5.	Input	:	Max : 2Vpp, Input Current: 1mA, Max: 3mA
6.	Input	:	Max : 2Vpp, Input Current: 1mA, Max: 3mA
7.	Prog		
8.	Input	:	Max : 2Vpp, Input Current: 1mA, Max: 3mA
9.	Vcc	:	12V
10.	Input	:	Max : 2Vpp, Input Current: 1mA, Max: 3mA
11.	Input	:	Max : 2Vpp, Input Current: 1mA, Max: 3mA
12.	Ground		
13.	Output	:	5.5Vpp, Min : 4.5Vpp
14.	Output	:	5.5Vpp, Min : 4.5Vpp
15.	Output	:	5.5Vpp, Min : 4.5Vpp
16.	Output	:	5.5Vpp, Min : 4.5Vpp
17.	Output	:	5.5Vpp, Min : 4.5Vpp
18.	Output	:	5.5Vpp, Min : 4.5Vpp
19.	Ground		
20.	Input	:	Max : 2Vpp, Input Current: 1mA, Max : 3mA

14.11.VPC3230D

14.11.1.General Description

The VPC 323xD is a high-quality, single-chip video front-end, which is targeted for 4:3 and 16:9, 50/60-Hz and 100/120 Hz TV sets. It can be combined with other members of the DIGIT3000 IC family (such as DDP 331x) and/or it can be used with 3rd-party products. The main features of the VPC 323xD are;
– high-performance adaptive 4H comb filter Y/C separator with adjustable vertical peaking
– multi-standard color decoder PAL/NTSC/SECAM including all substandards
– four CVBS, one S-VHS input, one CVBS output
– two RGB/YC $_r$ C $_b$ component inputs, one Fast Blank (FB) input
– integrated high-quality A/D converters and associated clamp and AGC circuits
– multi-standard sync processing
– linear horizontal scaling (0.25 ... 4), as well as non-linear horizontal scaling ‘Panorama-vision’
– PAL+ preprocessing
– line-locked clock, data and sync, or 656-output interface
– peaking, contrast, brightness, color saturation and tint for RGB/ YC $_r$ C $_b$ and CVBS/ S-VHS
– high-quality soft mixer controlled by Fast Blank
– PIP processing for four picture sizes (1/4, 1/9, 1/16 or 1/36 of normal size) with 8-bit resolution
– 15 predefined PIP display configurations and expert mode (fully programmable)
– control interface for external field memory
– I^2C-bus interface
– one 20.25-MHz crystal, few external components
– 80-pin PQFP package

14.11.2.Pin Connections and Short Descriptions

NC = not connected
LV = if not used, leave vacant
X = obligatory; connect as described in circuit diagram
SUPPLYA = 4.75...5.25 V, SUPPLYD = 3.15...3.45 V

Pin No. PQFP 80-pin	Pin Name	Type	Connection (if not used)	Short Description
1	B1/CB1IN	IN	VREF	Blue1/Cb1 Analog Component Input
2	G1/Y1IN	IN	VREF	Green1/Y1 Analog Component Input

3	R1/CR1IN	IN	VREF	Read1/Cr1 Analog Component Input
4	B2/CB2IN	IN	VREF	Blue2/Cb2 Analog Component Input
5	G2/Y2IN	IN	VREF	Green2/Y2 Analog Component Input
6	R2/CR2IN	IN	VREF	Read2/Cr2 Analog Component Input
7	ASGF		X	Analog Shield GND_F
8	FFRSTWIN	IN	LV or GND_D	FIFO Reset Write Input
9	V_{SUPCAP}	OUT	X	Digital Decoupling Circuitry Supply Voltage
10	V_{SUPD}	SUPPLYD	X	Supply Voltage, Digital Circuitry
11	GND_D	SUPPLYD	X	Ground, Digital Circuitry
12	GND_{CAP}	OUT	X	Digital Decoupling Circuitry GND
13	SCL	IN/OUT	X	I^2C Bus Clock
14	SDA	IN/OUT	X	I^2C Bus Data
15	RESQ	IN	X	Reset Input, Active Low
16	TEST	IN	GND_D	Test Pin, connect to GND_D
17	VGAV	IN	GND_D	VGAV Input
18	YCOEQ	IN	GND_D	Y/C Output Enable Input, Active Low
19	FFIE	OUT	LV	FIFO Input Enable
20	FFWE	OUT	LV	FIFO Write Enable
21	FFRSTW	OUT	LV	FIFO Reset Write/Read
22	FFRE	OUT	LV	FIFO Read Enable
23	FFOE	OUT	LV	FIFO Output Enable
24	CLK20	IN/OUT	LV	Main Clock output 20.25 MHz
25	GND_{PA}	OUT	X	Pad Decoupling Circuitry GND
26	V_{SUPPA}	OUT	X	Pad Decoupling Circuitry Supply Voltage
27	LLC2	OUT	LV	Double Clock Output
28	LLC1	IN/OUT	LV	Clock Output
29	V_{SUPLLC}	SUPPLYD	X	Supply Voltage, LLC Circuitry
30	GND_{LLC}	SUPPLYD	X	Ground, LLC Circuitry
31	Y7	OUT	GND_Y	Picture Bus Luma (MSB)
32	Y6	OUT	GND_Y	Picture Bus Luma
33	Y5	OUT	GND_Y	Picture Bus Luma
34	Y4	OUT	GND_Y	Picture Bus Luma
35	GND_Y	SUPPLYD	X	Ground, Luma Output Circuitry
36	V_{SUPY}	SUPPLYD	X	Supply Voltage, Luma Output Circuitry
37	Y3	OUT	GND_Y	Picture Bus Luma
38	Y2	OUT	GND_Y	Picture Bus Luma
39	Y1	OUT	GND_Y	Picture Bus Luma
40	Y0	OUT	GND_Y	Picture Bus Luma (LSB)
41	C7	OUT	GND_C	Picture Bus Chroma (MSB)
42	C6	OUT	GND_C	Picture Bus Chroma
43	C5	OUT	GND_C	Picture Bus Chroma
44	C4	OUT	GND_C	Picture Bus Chroma
45	V_{SUPC}	SUPPLYD	X	Supply Voltage, Chroma Output Circuitry
46	GND_C	SUPPLYD	X	Ground, Chroma Output Circuitry
47	C3	OUT	GND_C	Picture Bus Chroma
48	C2	OUT	GND_C	Picture Bus Chroma
49	C1	OUT	GND_C	Picture Bus Chroma
50	C0	OUT	GND_C	Picture Bus Chroma (LSB)
51	GND_{SY}	SUPPLYD	X	Ground Sync Pad Circuitry
52	V_{SUPSY}	SUPPLYD	X	Supply Voltage, Sync Pad Circuitry
53	INTLC	OUT	LV	Interlace Output
54	AVO	OUT	LV	Active Video Output
55	FSY/HC/HSYA	OUT	LV	Front Sync/ Horizontal Clamp Pulse/Front-End Horizontal Sync Output
56	MSY/HS	IN/OUT	LV	Main Sync/Horizontal Sync Pulse
57	VS	OUT	LV	Vertical Sync Pulse
58	FPDAT/VSYA	IN/OUT	LV	Front End/Back-End Data/Front-End Vertical Sync Output
59	V_{STBYY}	SUPPLYA	X	Standby Supply Voltage
60	CLK5	OUT	LV	CCU 5 MHz Clock Output
61	NC	-	LV or GND_D	Not Connected
62	XTAL1	IN	X	Analog Crystal Input
63	XTAL2	OUT	X	Analog Crystal Output
64	ASGF		X	Analog Shield GND_F
65	GND_F	SUPPLYA	X	Ground, Analog Front-End
66	VRT	OUTPUT	X	Reference Voltage Top, Analog

67	I2CSEL	IN	X	I^2C Bus Address Select
68	ISGND	SUPPLYA	X	Signal Ground for Analog Input, connect to GND_F
69	V_{SUPF}	SUPPLYA	X	Supply Voltage, Analog Front-End
70	VOUT	OUT	LV	Analog Video Output
71	CIN	IN	LV	Chroma/Analog Video 5 Input
72	VIN1	IN	VRT	Video 1 Analog Input
73	VIN2	IN	VRT	Video 2 Analog Input
74	VIN3	IN	VRT	Video 3 Analog Input
75	VIN4	IN	VRT	Video 4 Analog Input
76	V_{SUPAI}	SUPPLYA	X	Supply Voltage, Analog Component Inputs Front-End
77	GND_{AI}	SUPPLYA	X	Ground, Analog Component Inputs Front-End
78	VREF	OUTPUT	X	Reference Voltage Top, Analog Component Inputs Front-End
79	FB1IN	IN	VREF	Fast Blank Input
80	AISGND	SUPPLYA	X	Signal Ground for Analog Component Inputs, connect to GND_{AI}

14.12.TDA1308T

14.12.1.General Description

The TDA1308 is an integrated class AB stereo headphone driver contained in an SO8 or a DIP8 plastic package. The device is fabricated in a 1 mm CMOS process and has been primarily developed for portable digital audio applications. It gets its input from two analog audio outputs (DACA_L and DACA_R) of MSP3411G. The gain of the output is adjustable by the feedback resistor between the inputs and outputs.

14.12.2.Features

- Wide temperature range
- No switch ON/OFF clicks
- Excellent power supply ripple rejection
- Low power consumption
- Short-circuit resistant
- High performance
- high signal-to-noise ratio
- High slew rate
- Low distortion
- Large output voltage swing.

14.12.3.Pinning

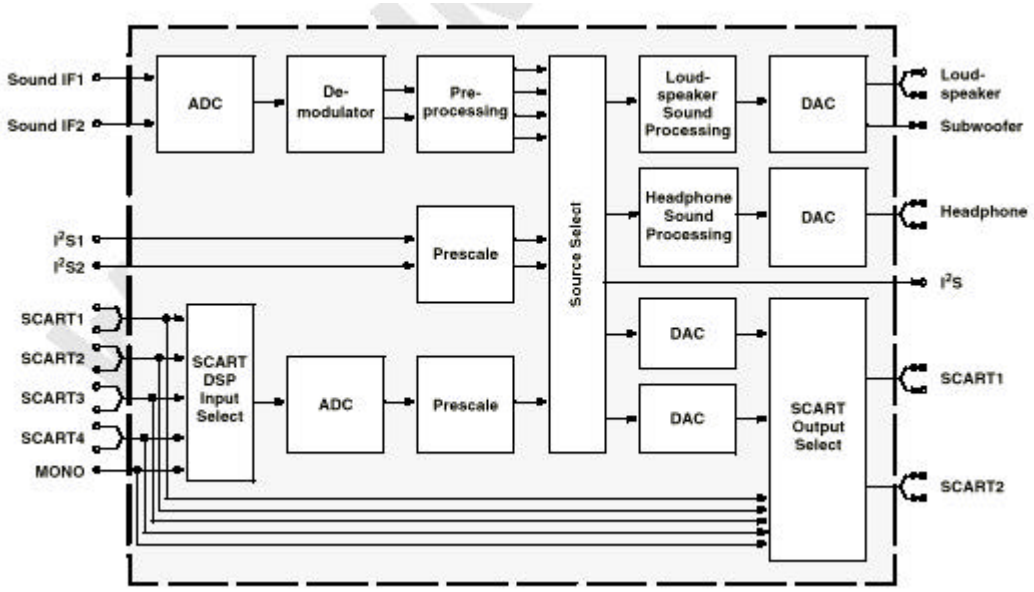
SYMBOL	PIN	DESCRIPTION
OUTA	1	Output A
INA(neg)	2	Inverting input A
INA(pos)	3	Non-inverting input A
V_{SS}	4	Negative supply
INB(pos)	5	Non-inverting input B
INB(neg)	6	Inverting input B
OUTB	7	Output B
V_{DD}	8	Positive supply

14.13.MSP34X1G (MSP3411G)

14.13.1.Description

The MSP 34x1G family of single-chip Mullet-standard Sound Processors covers the sound processing of all analog TV-Standards worldwide, as well as the NICAM digital sound standards. The full TV sound processing, starting with analog sound IF signal-in, down to processed analog AF-out, is performed on a single chip. Figure shows a simplified functional block diagram of the MSP34x1G. The MSP34x1G has all functions of the MSP34x0G with the addition of a virtual surround sound feature. Surround sound can be reproduced to a certain extent with two loudspeakers. The MSP34x1G includes our virtualizer algorithm “3D-PANORAMA” which has been approved by the Dolby 1) Laboratories for compliance with the "Virtual Dolby Surround" technology. In addition, the MSP34x1G includes the

“PANORAMA” algorithm. These TV sound processing ICs include versions for processing the multi-channel television sound (MTS) signal conforming to the standard recommended by the Broadcast Television Systems Committee (BTSC). The DBX noise reduction, or alternatively, Micronas Noise Reduction (MNR) is performed alignment free. Other processed standards are the Japanese FM-FM multiplex standard (EIA-J) and the FM Stereo Radio standard. Current ICs have to perform adjustment procedures in order to achieve good stereo separation for BTSC and EIA-J. The MSP34x1G has optimum stereo performance without any adjustments. All MSP 34xxG versions are pin and software downward compatible to the MSP 34xxD. MSP34x1G further simplifies controlling software. Standard selection requires a single I^2C transmission only. The MSP34x1G has built-in automatic functions: The IC is able to detect the actual sound standard automatically (Automatic Standard Detection). Furthermore, pilot levels and identification signals can be evaluated internally with subsequent switching between mono/stereo/bilingual; no I^2C interaction is necessary (Automatic Sound Selection).



14.13.2.Features

3D-PANORAMA virtualizer (approved by Dolby Laboratories) with noise generator
PANORAMA virtualizer algorithm
Standard Selection with single I^2C transmission
Automatic Standard Detection of terrestrial TV standards/Automatic Carrier Mute function
Automatic Sound Selection (mono/stereo/bilingual), new registers MODUS, STATUS
Two selectable sound IF (SIF) inputs
Interrupt output programmable (indicating status change)
Loudspeaker / Headphone channel with volume, balance, bass, treble, loudness
Loudspeaker channel with MDB (Micronas Dynamic Bass)
AVC: Automatic Volume Correction
Subwoofer output with programmable low-pass and complementary high-pass filter
5-band graphic equalizer for loudspeaker channel
Spatial effect for loudspeaker channel; processing of all deemphasis filtering
Four Stereo SCART (line) inputs, one Mono input; two Stereo SCART outputs
Complete SCART in/out switching matrix
Two I^2S inputs; one I^2S output
All analog FM-Stereo A2 and satellite standards
All analog Mono sound carriers including AM-SECAM L
Simultaneous demodulation of (very) high-deviation FM-Mono and NICAM
Adaptive deemphasis for satellite (Wegener-Panda, acc. to ASTRA specification)
ASTRA Digital Radio (ADR) together with DRP 3510A
All NICAM standards
Korean FM-Stereo A2 standard

14.13.3.Pin connections

NC = not connected; leave vacant
LV = if not used, leave vacant
X = obligatory; connect as described in circuit diagram
DVSS: if not used, connect to DVSS
AHVSS: connect to AHVSS

Pin No.					Pin Name	Type	Connection (if not used)	Short Description
PLCC 68-pin	PSDIP 64-pin	PSDIP 52-pin	PQFP 80-pin	PLQFP 64-pin				
1	16	14	9	8	ADR_WS	OUT	LV	ADR word strobe
2	-	-	-	-	NC		LV	Not connected
3	15	13	8	7	ADR_DA	OUT	LV	ADR Data Output
4	14	12	7	6	I2S_DA_IN1	IN	LV	I²S1 data input
5	13	11	6	5	I2S_DA_OUT	OUT	LV	I²S data output
6	12	10	5	4	I2S_WS	IN/OUT	LV	I²S word strobe
7	11	9	4	3	I2S_CL	IN/OUT	LV	I²S clock
8	10	8	3	2	I2C_DA	IN/OUT	X	I²C data
9	9	7	2	1	I2C_CL	IN/OUT	X	I²C data
10	8	-	1	64	NC		LV	Not connected
11	7	6	80	63	STANDBYQ	IN	X	Stand-by (low-active)
12	6	5	79	62	ADR_SEL	IN	X	I²C bus address select
13	5	4	78	61	D_CTR_I/O_0	IN/OUT	LV	D_CTR_I/O_0
14	4	3	77	60	D_CTR_I/O_1	IN/OUT	LV	D_CTR_I/O_1
15	3	-	76	59	NC		LV	Not connected
16	2	-	75	58	NC		LV	Not connected
17	-	-	-	-	NC		LV	Not connected
18	1	2	74	57	AUD_CL_OUT	OUT	LV	Audio clock output (18.432 MHz)
19	64	1	73	56	TP		LV	Test pin
20	63	52	72	55	XTAL_OUT	OUT	X	Crystal oscillator
21	62	51	71	54	XTAL_IN	IN	X	Crystal oscillator
22	61	50	70	53	TESTEN	IN	X	Test pin
23	60	49	69	52	ANA_IN2+	IN	AVSS via 56 pF/LV	IF Input 2 (can be left vacant, only if IF input 1 is also not in use)
24	59	48	68	51	ANA_IN-	IN	AVSS via 56 pF/LV	IF common (can be left vacant, only if IF input 1 is also not in use)
25	58	47	67	50	ANA_IN1+	IN	LV	IF input 2
26	57	46	66	49	AVSUP		X	Analog power supply 5v
-	-	-	65	-	AVSUP		X	Analog power supply 5v
-	-	-	64	-	NC		LV	Not connected
-	-	-	63	48	NC		LV	Not connected
27	56	45	62	48	AVSS		X	Analog ground
-	-	-	61	-	AVSS		X	Analog ground
28	55	44	60	47	MONO_IN	IN	LV	Mono input
-	-	-	59	-	NC		LV	Not connected
29	54	43	58	46	VREFTOP		X	Reference voltage IF A/D converter
30	53	42	57	45	SC1_IN_R	IN	LV	SCART 1 input, right
31	52	41	56	44	SC1_IN_L	IN	LV	SCART 1 input, left
32	51	-	55	43	ASG		AHVSS	Analog Shield Ground
33	50	40	54	42	SC2_IN_R	IN	LV	SCART 2 input, right
34	49	39	53	41	SC2_IN_L	IN	LV	SCART 2 input, left
35	48	-	52	40	ASG		AHVSS	Analog Shield Ground
36	47	38	51	39	SC3_IN_R	IN	LV	SCART 3 input, right
37	46	37	50	38	SC3_IN_L	IN	LV	SCART 3 input, left
38	45	-	49	37	ASG		AHVSS	Analog Shield Ground
39	44	-	48	36	SC4_IN_R	IN	LV	SCART 4 input, right
40	43	-	47	35	SC4_IN_L	IN	LV	SCART 4 input, left
41	-	-	46	-	NC		LV or AHVSS	Not connected
42	42	36	45	34	AGNDC		X	Analog reference voltage
43	41	35	44	33	AHVSS		X	Analog ground
-	-	-	43	-	AHVSS		X	Analog ground
-	-	-	42	-	NC		LV	Not connected
-	-	-	41	-	NC		LV	Not connected
44	40	34	40	32	CAPL_M		X	Volume capacitor MAIN
45	39	33	39	31	AHVSUP		X	Analog power supply 8V

46	38	32	38	30	CAPL_A		X	Volume capacitor AUX
47	37	31	37	29	SC1_OUT_L	OUT	LV	SCART output 1, left
48	36	30	36	28	SC1_OUT_R	OUT	LV	SCART output 1, right
49	35	29	35	27	VREF		X	Reference ground 1
50	34	28	34	26	SC2_OUT_L	OUT	LV	SCART output 2, left
51	33	27	33	25	SC2_OUT_R	OUT	LV	SCART output 2, right
52	-	-	32	-	NC		LV	Not connected
53	32	-	31	24	NC		LV	Not connected
54	31	26	30	23	DACM_SUB	OUT	LV	Subwoofer output
55	30	-	29	22	NC		LV	Not connected
56	29	25	28	21	DACM_L	OUT	LV	Loudspeaker out, left
57	28	24	27	20	DACM_R	OUT	LV	Loudspeaker out, right
58	27	23	26	19	VREF2		X	Reference ground 2
59	26	22	25	18	DACA_L	OUT	LV	Headphone out, left
60	25	21	24	17	DACA_R	OUT	LV	Headphone out, right
-	-	-	23	-	NC		LV	Not connected
-	-	-	22	-	NC		LV	Not connected
61	24	20	21	16	RESETQ	IN	X	Power-on-reset
62	23	-	20	15	NC		LV	Not connected
63	22	-	19	14	NC		LV	Not connected
64	21	19	18	13	NC		LV	Not connected
65	20	18	17	12	I2S_DA_IN2	IN	LV	I²S2-data input
66	19	17	16	11	DVSS		X	Digital ground
-	-	-	15	-	DVSS		X	Digital ground
-	-	-	14	-	DVSS		X	Digital ground
67	18	16	13	10	DVSUP		X	Digital power supply 5V
-	-	-	12	-	DVSUP		X	Digital power supply 5V
-	-	-	11	-	DVSUP		X	Digital power supply 5V
68	17	15	10	9	ADR_CL	OUT	LV	ADR clock

14.14.TL431

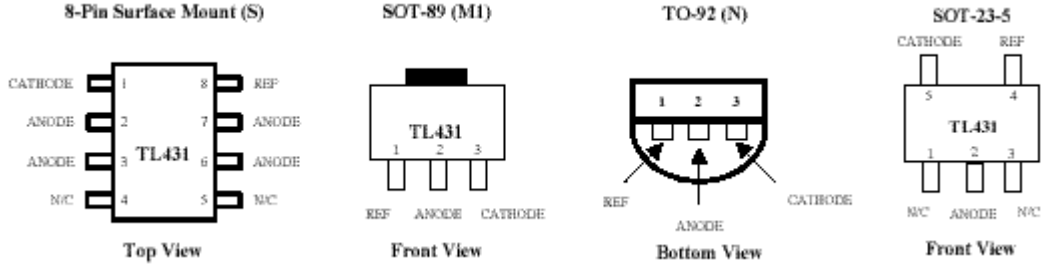
14.14.1.Description

The TL431 is a 3-terminal adjustable shunt voltage regulator providing a highly accurate 1 % band gap reference. TL431 acts as an open-loop error amplifier with a 2.5V temperature compensation reference. The TL431 thermal stability, wide operating current (150mA) and temperature range (0.to 105.makes it suitable for all variety of application that are looking for a low cost solution with high performance. The output voltage may be adjusted to any value between VREF and 36 volts with two external resistors. The TL431 is operating in full industrial temperature range of 0°C to 105°C. The TL431 is available in TO-92, SO-8, SOT-89 and SOT23-5 packages.

14.14.2.Features

- Trimmed Band gap to 1%
- Wide Operating Current 1mA to 150mA
- Extended Temperature Range 0. °C to 105.°C
- Low Temperature Coefficient 30 ppm /°C
- Offered in TO-92, SOIC, SOT-89, SOT-23-5
- Improved Replacement in Performance for TL431
- Low Cost Solution

14.14.3.Pin Configurations



14.15.DRX3960A

14.15.1.Introduction

The Digital Receiver Front-end DRX 3960A performs the entire multi-standard Quasi Split Sound (QSS) TV IF processing, AGC, video demodulation, and generation of the second sound IF (SIF) with only one SAW filter. The IC is designed for applications in TV sets, VCRs, PC cards, and TV tuners. The alignment-free DRX 3960A needs no special external components. All control functions and status registers are accessible via I²C bus interface. Therefore, it simplifies the design of high-quality, highly standardized IF stages. Due to its mixed signal structure and the digital demodulation, the IC offers unique features and is prepared for digital TV.

14.15.2.Features

– Multi-standard QSS IF processing with a single SAW
– Highly reduced amount of external components (no tank circuit, no potentiometers, no SAW switching)
– Programmable IF frequency (38.9 MHz, 45.75 MHz, 32.9 MHz, 36.125 MHz etc.)
– Digital IF processing for the following standards: B/G, D/K, I, L/L', and M/N
– Standard specific digital post filtering
– Standard specific digital video/audio splitting
– Standard specific digital picture carrier recovery:
– alignment-free
– Quartz-stable and accurate
– Stable frequency lock at 100% modulation and over modulation up to 115%
– Quartz-accurate AFC information
– Programmable standard specific digital group delay equalizing
– Automatically frequency-adjusted Nyquist slope, therefore optimal picture and sound performance over complete lock in frequency range
– Standard specific digital AGC and delayed tuner AGC with programmable tuner Take Over Point
– Fast AGC due to linear structure
– Adaptive back porch control, therefore fast positive modulation AGC
– No sound traps needed at video output
– Second SIF output with standard dependent pre-filtering and amplitude controlled output level
– Optimal sound SNR due to carrier recovery without quadrature distortions
– FM radio capability without external components and with standard TV tuner
– Prepared for digital TV (DVB-C, DVB-T, ATSC)
– I^2C bus interface

14.15.3.Pin connection and short descriptions

NC = not connected, leave vacant
DVSS = if not used, connect to DVSS
X = obligatory; connect as described in circuit diagram
LV = if not used, leave vacant
AHVSS = connect to AHVSS

Pin no PLCCK 68 pin	Pin name	Type	Supply Voltage	Connection (if not used)	Short description
1	AVSS_ADC			X	Analog Ground for ADC
2	AVDD_ADC			X	Analog Supply for ADC (+5V)
3	ANASTX	I/O	AVDD_FE8	GND	Test pin
4	ANASTY	I/O	AVDD_FE8	GND	Test pin
5	AVDD_FE8			X	2nd analog supply for the front-end
6	AVSS_FE8			X	2nd analog ground for the front-end
7	AVSS_FE40				1st analog ground for the front-end
8	IFINX	IN	AVDD_FE40	X	IF Input
9	AVDD_FE40			X	1st analog supply for the front-end
10	IFINY	IN	AVDD_FE40	X	IF Input
11	AVSS_FE40			X	1st analog ground for the front-end
12	AVDD_SYN			X	Analog supply for synthesizer (+5V)
13	AVSS_SYN			X	Analog ground for synthesizer
14	SHIELD	IN		X	Shield GND
15	TEST0	IN	AVDD_DAC	GND	Test pin
16	TEST1	IN	AVDD_DAC	GND	Test pin
17	TEST2	IN	AVDD_DAC	GND	Test pin

18	CVBS	OUT	AVDD_DAC	X	CVBS Output
19	REF_SW	IN	AVDD_DAC	X	Reference frequency switch
20	SIF	OUT	AVDD_DAC	X	2nd SIF output
21	AVDD_DAC			X	DAC supply (+5V)
22	AVSS_DAC			X	DAC ground
23	TEST_EN	IN	DVDD	GND	Test enable
24	RESETQ	IN	DVDD	X	Reset
25	I2C_SDC	I/O	DVDD	X	I2C data
26	I2C_SCL	I/O	DVDD	X	I2C clock
27	DVDD_CAP			X	Digital supply capacitor
28	DVDD			X	Digital supply (+3.3V)
29	DVSS			X	Digital ground
30	DVSS_CAP			X	Digital capacitor ground
31	PORT0	OUT	DVDD	LV	Digital output port
32	PORT1	OUT	DVDD	LV	Digital output port
33	TUNER_AGC	OUT	DVDD	X	Tuner AGC current output
34	PORT2	OUT	DVDD	LV	Digital output port
35	PORT3	OUT	DVDD	LV	Digital output port
36	PORT4	OUT	DVDD	LV	Digital output port
37	ADR_SEL	IN	DVDD	X	Address select
38	PORT5	OUT	DVDD	LV	Digital output port
39	DVDD_ADC			X	Digital supply for ADC (+3.3V)
40	DVSS_ADC			X	Digital ground for ADC
41	XTAL_IN	IN	AVDD_ADC	X	Crystal oscillator
42	XTAL_OUT	I/O	AVDD_ADC	X	Crystal oscillator/external reference frequency
43	VREF		AVDD_ADC	X	ADC Reference voltage
44	SGND		AVDD_ADC	X	ADC Reference ground

14.16.LM7808

14.16.1.Description

The L7800 series of three-terminal positive regulators is available in TO-220 TO-220FP TO-3 and D 2 PAK packages and several fixed output voltages, making it useful in a wide range of applications. These regulators can provide local on-card regulation, eliminating the distribution problems associated with single point regulation. Each type employs internal current limiting, thermal shutdown and safe area protection, making it essentially indestructible. If adequate heat sinking is provided, they can deliver over 1A output current. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

14.16. 2.Features

Output Current Up To 1.5 A
Output Voltages of 5; 5.2; 6; 8; 8.5; 9; 12; 15; 18; 24V
Thermal Over load protection
Short Circuit Protection
Output Transition SOA Protection

14.17.BDX53BFI

14.17.1.Description

The BDX53BFI is silicon epitaxial-base NPN power transistor in monolithic Darlington configuration and are mounted in ISOWATT220 plastic package. It is intended for use in hammer drivers, audio amplifiers and other medium power linear and switching applications. The complementary PNP type is the BDX54BFI.

14.17.2.Applications

General purpose switching and amplifier
Linear and switching industrial equipment

14.18.TDA8177F

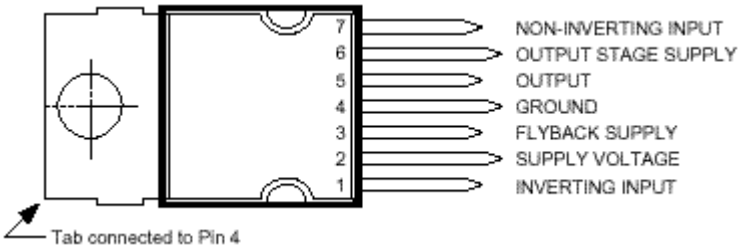
14.18.1.Description

Designed for monitors and high performance TVs, the TDA8177F vertical deflection booster can handle flyback voltage up to 70V. More than this it is possible to have a flyback voltage, which is more than the double of the supply (Pin 2). This allows to decrease the power consumption or to decrease the flyback time for a given supply voltage. The TDA8177F operates with supplies up to 35V and provides up to 3APP output current to drive the yoke.

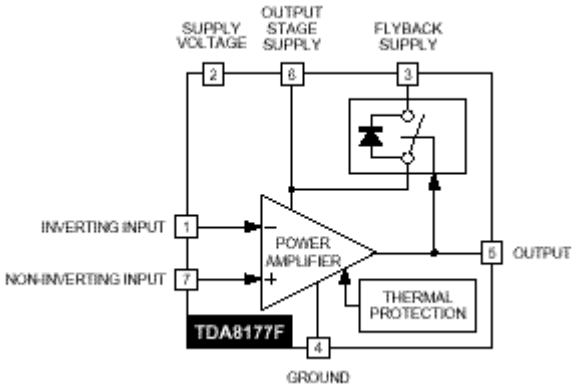
14.18.2.Features

Power Amplifier
Thermal Protection
Output Current Up To 3.0APP
Flyback Voltage Up To 70V (on Pin 5)
Suitable For Dc Coupling Application
External Flyback Supply

14.18.3.Pin connections



14.18.4.Block Diagram



14.19.LM1086

14.19.1.Description

The LM1086 is a series of low dropout positive voltage regulators with a maximum dropout of 1.5V at 1.5A of load current. It has the same pin-out as National Semiconductor's industry standard LM317. The LM1086 is available in an adjustable version, which can set the output voltage with only two external resistors. It is also available in five fixed voltages: 2.5V, 2.85V, 3.3V, 3.45V and 5.0V. The fixed versions integrate the adjust resistors. The LM1086 circuit includes a zener trimmed band-gap reference, current limiting and thermal shutdown.

14.19.2.Features

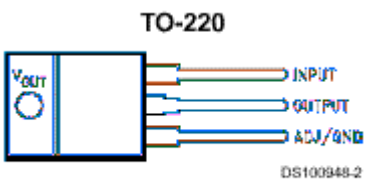
Available in 2.5V, 2.85V, 3.3V, 3.45V, 5V and Adjustable Versions
Current Limiting and Thermal Protection

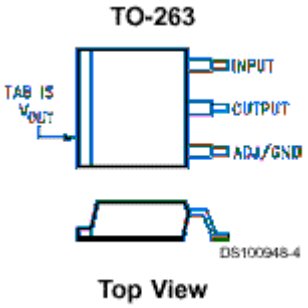
Output Current 1.5A
Line Regulation 0.015% (typical)
Load Regulation 0.1% (typical)

14.19.3.Applications

SCSI-2 Active Terminator
High Efficiency Linear Regulators
Battery Charger
Post Regulation for Switching Supplies
Constant Current Regulator
Microprocessor Supply

14.19.4.Connection Diagrams





14.20.MC44608

14.20.1.Description

The MC44608 is a high performance voltage mode controller designed for off–line converters. This high voltage circuit that integrates the start–up current source and the oscillator capacitor, requires few external components while offering a high flexibility and reliability. The device also features a very high efficiency stand–by management consisting of an effective Pulsed Mode operation. This technique enables the reduction of the stand–by power consumption to approximately 1W while delivering 300mW in a 150W SMPS.

• Integrated Start–Up Current Source
• Lossless Off–Line Start–Up
• Direct Off–Line Operation
• Fast Start–Up

14.20.2.General Features

• Flexibility
• Duty Cycle Control
• Under voltage Lockout with Hysteresis
• On Chip Oscillator Switching Frequency 40, or 75kHz
• Secondary Control with Few External Components

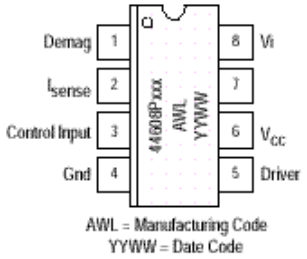
Protections

• Maximum Duty Cycle Limitation
• Cycle by Cycle Current Limitation
• Demagnetization (Zero Current Detection) Protection
• “Over VCC Protection” Against Open Loop
• Programmable Low Inertia Over Voltage Protection Against Open Loop
• Internal Thermal Protection

GreenLine™ Controller

• Pulsed Mode Techniques for a Very High Efficiency Low Power Mode
• Lossless Startup
• Low dV/dT for Low EMI Radiations

14.20.3.Pin Connections



14.20.4.Pin Function description

Pin	Name	Description
1	Demag	The Demag pin offers 3 different functions: Zero voltage crossing detection (50mV), 24mA current detection and 120mA current detection. The 24mA level is used to detect the secondary reconfiguration status and the 120mA level to detect an Over Voltage status called Quick OVP.
2	ISENSE	The Current Sense pin senses the voltage developed on the series resistor inserted in the source of the power MOSFET. When I sense reaches 1V, the Driver output (pin 5) is disabled. This is known as the Over Current Protection function. A 200mA current source is flowing out of the pin 3 during the start–up phase and during the switching phase in case of the Pulsed Mode of operation. A resistor can be inserted between the sense resistor and the pin 3; thus a programmable peak current detection can be performed during the SMPS stand–by mode.
3	Control Input	A feedback current from the secondary side of the SMPS via the opto–coupler is injected into this pin. A resistor can be connected between this pin and GND to allow the programming of the Burst duty cycle during the Stand–by mode.
4	Ground	This pin is the ground of the primary side of the SMPS.
5	Driver	The current and slew rate capability of this pin are suited to drive Power MOSFETs.
6	VCC	This pin is the positive supply of the IC. The driver output gets disabled when the voltage becomes higher than 15V and the operating range is between 6.6V and 13V. An intermediate voltage level of 10V creates a disabling condition called Latched Off phase.
7		This pin is to provide isolation between the Vi pin 8 and the VCC pin 6.
8	Vi	This pin can be directly connected to a 500V voltage source for start–up function of the IC. During the Start–up phase a 9 mA current source is internally delivered to the VCC pin 6 allowing a rapid charge of the VCC capacitor. As soon as the IC starts–up, this current source is disabled.

14.21.TCET1102G

14.21.1.Description

The TCET110/ TCET2100/ TCET4100 consists of a phototransistor optically coupled to a gallium arsenide infrared-emitting diode in a 4-lead up to 16-lead plastic dual inline package. The elements are mounted on one lead frame using a **coplanar technique**, providing a fixed distance between input and output for highest safety requirements.

14.21.2.Applications

Circuits for safe protective separation against electrical shock according to safety class II (reinforced isolation):
For appl. class I – IV at mains voltage =300 V
For appl. class I – III at mains voltage =600 V
According to VDE 0884, table 2, suitable for: **Switch-mode power supplies, line receiver, computer peripheral interface, microprocessor system interface.**

14.21.3.Features

VDE 0884 related features:
Rated impulse voltage (transient overvoltage) V_{IOTM} = 8 kV peak
Isolation test voltage (partial discharge test voltage) V_{pd} = 1.6 kV
Rated isolation voltage (RMS includes DC) V_{IOWM} = 600 V_{RMS} (848 V peak)
Rated recurring peak voltage (repetitive) V_{IORM} = 600 V_{RMS}

General features:
CTR offered in 9 groups
Isolation materials according to UL94-VO
Pollution degree 2 (DIN/VDE 0110 / resp. IEC 664)
Climatic classification 55/100/21 (IEC 68 part 1)
Special construction: Therefore, extra low coupling capacity of typical 0.2pF, high **C**ommon **M**ode **R**ejection
Low temperature coefficient of CTR
G = Leadform 10.16 mm; provides creepage distance > 8 mm, for TCET2100/ TCET4100 optional; suffix letter 'G' is not marked on the optocoupler
Coupling System U

14.22.TDA7480L

14.22.1.Description

The TDA7480L is an audio class-D amplifier assembled in Power DIP package specially de-signed for high efficiency applications mainly for TV and Home Stereo sets.

14.22.2.Features

10W Output Power: R_L = 8Ω/4Ω; THD = 10%
High Frequency
No Heatsink
Split Supply
Overvoltage Protection
St-By And Mute Features
Short Circuit Protection
Thermal Overload Protection

14.22.3.Pin Functions

Number	Name	Function
1	$-V_{CC}$	NEGATIVE SUPPLY.
2	$-V_{CC}$	NEGATIVE SUPPLY.
3	$-V_{CC}$	NEGATIVE SUPPLY.
4	OUT	PWM OUTPUT
5	BOOTDIODE	BOOTSTRAP DIODE ANODE
6	BOOT	BOOTSTRAP CAPACITOR
7	NC	NOT CONNECTED
8	FEEDCAP	FEEDBACK INTEGRATING CAPACITANCE
9	FREQUENCY	SETTING FREQUENCY RESISTOR
10	SGN-GND	SIGNAL GROUND
11	IN	INPUT
12	ST-BY-MUTE	ST-BY/ MUTE CONTROL PIN
13	NC	NOT CONNECTED
14	$+V_{CC}$ SIGN	POSITIVE SIGNAL SUPPLY
15	V_{REG}	10V INTERNAL REGULATOR
16	$+V_{CC}$ POW	POSITIVE POWER SUPPLY
17	$-V_{CC}$	NEGATIVE SUPPLY (TO BE CONNECTED TO PIN 16 VIA C5)
18	$-V_{CC}$	NEGATIVE SUPPLY
19	$-V_{CC}$	NEGATIVE SUPPLY
20	$-V_{CC}$	NEGATIVE SUPPLY

14.23.SAA3010T

14.23.1.Description

The SAA3010 is intended as a general purpose (RC-5) infrared remote control system for use where a low voltage supply and a large debounce time are expected. The device can generate 2048 different commands and utilizes a keyboard with a single pole switch for each key. The commands are arranged so that 32 systems can be addressed, each system containing 64 different commands. The circuit response to legal (one key pressed at a time) and illegal (more than one key pressed at a time) keyboard operation is specified in the section "Keyboard operation".

14.23.2.Features

Low voltage requirement
Biphase transmission technique
Single pin oscillator
Test mode facility

14.23.3.Pinning

Pin	Mnemonic	Function
1	X7 (IPU)	sense input from key matrix
2	SSM (I)	sense mode selection input
3	Z0-Z3 (IPU)	sense inputs from key matrix
7	MDATA (OP3)	generated output data modulated with 1/12 the oscillator frequency at a 25% duty factor
8	DATA (OP3)	generated output information
9-13	DR7-DR3 (ODN)	Scan drivers
14	VSS	Ground (0V)
15-17	DR-2-DR0 (ODN)	Scan drivers
18	OSC (I)	Oscillator input
19	TP2 (I)	test point 2
20	TP1 (I)	Test point 1
21-27	X0-X6 (IPU)	Sense inputs from key matrix
28	VDD(I)	Voltage supply

Note:
(I): Input,
(IPU): input with p-channel pull-up transistor,
(ODN): output with open drain n-channel transistor
(OD3): output 3-state

15.AK52 CHASSIS MANUAL ADJUSTMENTS PROCEDURE

15.1.PRELIMINARY

Before starting with the alignment procedure, make sure that all the potentiometers on the chassis and also screen and focus pots are in the medium position.

15.2.SYSTEM VOLTAGE ADJUSTMENTS

Inputs AC power (220V 50Hz)
PAL B/G test pattern via RF
(PAL I test pattern for PAL I TV's, SECAM D/K pattern, SECAM L/L'/K' TVs.)
Outputs Digital voltmeter to anode of D110.
Display System voltage
Action Apply power. Check that the stand-by Led lights.
Select TV mode and tune to the applied test pattern via local test keyboard.
Chassis should start normally.
Adjust all analog controls (volume, bass, treble, brightness, contrast, colour) to minimum settings.
Adjust VR127 according to the following different type of CRTs.

SYSTEM VOLTAGE	TYPE OF CRT
135V±0.5V	PHILIPS A66EAK552X54
135V±0.5V	PHILIPS A66EAK071X54
135V±0.5V	VIDEOCOLOR A66ECY13X12
135V±0.5V	PHILIPS W66ESF002X44

15.3.AFC ADJUSTMENTS

Inputs AC power
38.9 Mhz test pattern for PAL B/G, PAL-SECAM B/G or 39.5 MHz test pattern for PAL I model (90dBmV) to Z403 SAW filter input terminals 1 and 2.
Outputs Digital voltmeter to AFC point (pin22 of IC401)
Display AFC Voltage.
Action Adjust VL401 for 2.5±0.1 Volts. TV should automatically tune to a station when search tuning is activated.

15.4.FOCUS ADJUSTMENTS

Inputs AC power
PAL B/G test pattern via RF input.
Outputs Picture tube drive.
Display Picture
Action Select TV mode and tune to the signal.
Adjust focus potantiometer (the upper pot on the rear side of the FBT transformer) for optimum focusing drive.

15.5.SCREEN ADJUSTMENTS

Inputs AC power
PAL B/G Colour Bar test pattern via RF
Outputs 1/100 Oscilloscope probe to RGB cathodes on CRT baseboard.
NOTE: Ground pin of probe will be connected to 1st pin (GND) of the CRT socket.
Display RGB ratio
Action Select PAL B/G Colour bar pattern using the local test keyboard and the user remote control unit.
Adjust all control functions (brightness, colour and contrast) to minimum settings.
Measure the most sensitive cathode
Adjust the screen potentiometer (lower pot on the rear side of FBT transformer) until cathode voltage becomes 150V.

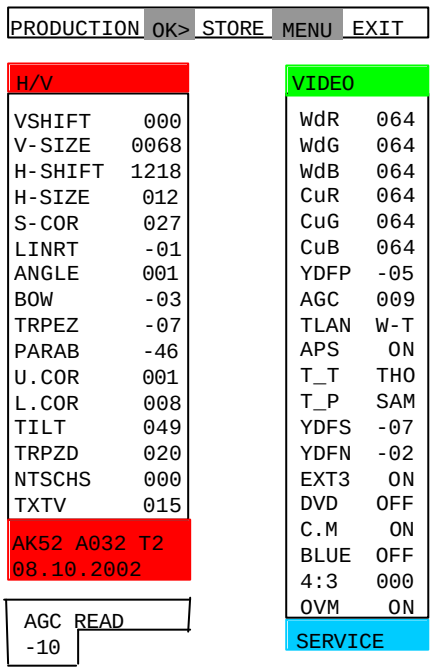
15.6.IF ADJUSTMENT FOR L' MODE

Inputs AC power
38.9 MHz test pattern for PAL B/G, PAL-SECAM B/G or 39.5 MHz test pattern for PAL I model. (90dBmV) to Z403 SAW filter input terminals 1 and 2.
Outputs Digital Voltmeter to AFC point. (pin22 of IC401)
Digital Voltmeter to AFC_L point. (pin14 of IC401
Display AFC Voltage.
Action Firstly adjust VL401 for 2.5±0.1 Volts. TV should automatically tune to a station when search tuning is activated.
Adjust VR401 for 2.5±0.1 Volts at the AFC_L point.

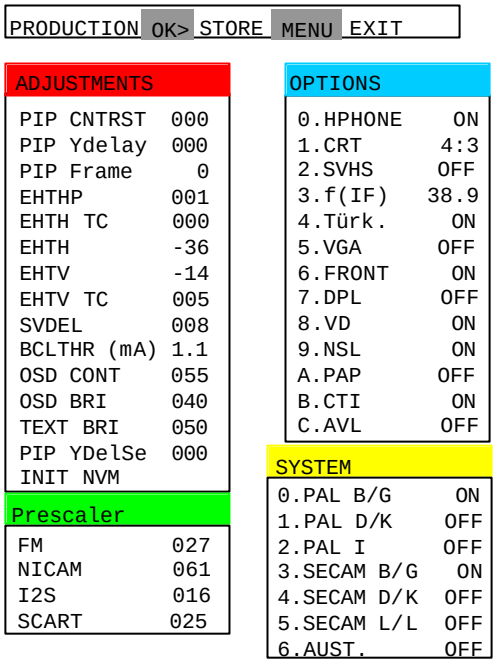
16.AK52 CHASSIS PRODUCTION SERVICE MODE ADJUSTMENTS

16.1.PRELIMINARY

All system, geometry and white balance alignments are performed in production service mode. Before starting the production mode alignments, make sure that all manual adjustments are done correctly. To start production mode alignments enter the MAIN MENU and then press the digits 1, 6, 7 and 5 respectively. The following first menu appears on the screen. Production mode values will appear on the screen.



First page



Second Page

SERVICE MENU

Production mode groups will be displayed with different colours of headlines, so in order to access a production alignment group press the colour button of the related group on the remote control transmitter.

- RED BUTTON is pressed to access H/V menu.
- GREEN BUTTON is pressed to access VIDEO adjust menu.
- BLUE BUTTON is pressed to go to the next page of the service menu.
- YELLOW BUTTON is used to adjust system parameters on the second page of the service menu.

After selecting one of the production service mode groups, you can access its items by pressing ? /? buttons. Selected parameter will be highlighted. Inorder to change the selected parameter, use ? / ? buttons. Inorder to switch between other group of items press the colour key of this groups headline.
To store the settings press OK button. To exit the service menu press MENU button.
Entire service menu parameters of AK52 CHASSIS are listed below.

16.2.H/V (HORIZONTAL AND VERTICAL GEOMETRY ALIGNMENTS)

Switch the program to crosshatch test pattern. Press RED button to access this group of item. Select the parameter by pressing up/down buttons. Adjust the parameter by pressing left/right buttons. Store the settings by pressing OK button. Switch the another parameter group by pressing the colour button of the related coloured headline of that group. Exit production mode by pressing the MENU button on the remote control.

V-SHIFT

Change Vertical Shift by pressing Left/Right buttons till the test pattern is vertically centered. Horizontal line at the center of the test pattern is in equal distance both to upper and lower side of the picture tube.

Check and readjust V-SHIFT item if the adjustment becomes improper after some other geometric adjustments are done.

Min. Value:	-128
Max. Value:	127
Recommended Value:	000

V-SIZE

Change Vertical Size by pressing Left/Right buttons till horizontal black lines on both the upper and lower part of the test pattern become very close to the upper and lower horizontal sides of picture tube and nearly about to disappear. Check and readjust V-SIZE item if the adjustment becomes improper after some other geometric adjustments are done.

Min. Value:	-128
Max. Value:	127
Recommended Value:	068

H-SHIFT

Change Horizontal Shift by pressing Left/Right buttons till the the test pattern is horizontally in equal distance both to right and left sides of the picture tube. Check and readjust H-SHIFT item if the adjustment becomes improper after some other geometric adjustments are done.

Min. Value:	0000
Max. Value:	1295
Recommended Value:	1218

H-SIZE

Change Horizontal Size by pressing Left/Right buttons till no under-scan condition will happen, i.e. no white bars on the left and right side of the test pattern will be visible nor picture will be so wide. Check and readjust H-SIZE item if the adjustment becomes improper after some other geometric adjustments are done.

Min. Value:	-128
Max. Value:	127
Recommended Value:	012

S-COR

Change S-Correction by pressing Left/Right buttons till the size of squares on both the upper and lower part of test pattern become equal to the squares laying on the vertical center of the test pattern. Check and readjust S-COR item if the adjustment becomes improper after some other geometric adjustments are done.

Min. Value:	-128
Max. Value:	127
Recommended Value:	027

LINRT

Change Linearity by pressing Left/Right buttons till all the size of squares of the test pattern become in equal size from the top of the screen to its bottom of the whole screen. Check and readjust LINRT item if the adjustment becomes improper after some other geometric adjustments are done. (especially after than S-COR adjustment)

Min. Value:	-128
Max. Value:	127
Recommended Value:	-01

ANGLE

Change Angle by pressing Left/Right buttons till the vertical lines of the crosshatch pattern become completely perpendicular to horizontal lines without any angle of vertical deviation. Check and readjust ANGLE item if the adjustment becomes improper after some other geometric adjustments are done.

Min. Value:	-128
Max. Value:	127
Recommended Value:	001

BOW

Change Bow by pressing Left/Right buttons till the vertical lines especially ones close to the left and right sides will of equal and symmetrical bending, i.e. they together will neither be towards left side nor right side. Check and readjust BOW item if the adjustment becomes improper after some other geometric adjustments are done.

Min. Value:	-128
Max. Value:	127
Recommended Value:	-03

TRPEZ

Change Trapezium by pressing Left/Right buttons till vertical lines, especially lines at the sides of the picture frame became parallel to the both sides of picture tube as close as possible. Check and readjust TRPEZ item if the adjustment becomes improper after some other geometric adjustments are done.

Min. Value:	-128
Max. Value:	127
Recommended Value:	-07

PARAB

Change Parabol by pressing Left/Right buttons till vertical lines close to the both sides of the picture frame become parallel to vertical sides of picture tube without any bending to left or to right side of the screen. Check and readjust PARAB item if the adjustment becomes improper after some other geometric adjustments are done.

Min. Value:	-128
Max. Value:	127
Recommended Value:	-46

U.COR

Change Upper Correction by pressing Left/Right buttons till vertical lines at the upper corners of the picture frame become vertical and parallel to vertical corner sides of picture tube. Check and readjust U.COR item if the adjustment becomes improper after some other geometric adjustments are done.

Min. Value:	-128
Max. Value:	127
Recommended Value:	001

L.COR

Change Lower Correction by pressing Left/Right buttons till vertical lines at the lower corners of the picture frame become vertical and parallel to vertical corner sides of picture tube. Check and readjust L.COR item if the adjustment becomes improper after some other geometric adjustments are done.

Min. Value:	-128
Max. Value:	127
Recommended Value:	008

TILT

This adjustment only works when the TV has rotation option. Change TILT by pressing Left/Right buttons to rotate the complete raster clock-wise and counter clock-wise depending on the CRT. Check and readjust TRPEZ item if the adjustment becomes improper after some other geometric adjustments are done.

Min. Value:	000
Max. Value:	063
Recommended Value:	049

TRPZD

Not used for this model.

NTSCHS

Change NTSC horizontal size by pressing Left/Right buttons to adjust till no under-scan condition will happen, i.e. no white bars on the left and right side of the NTSC test pattern will be visible nor picture will be so wide. Check and readjust TRPEZ item if the adjustment becomes improper after some other geometric adjustments are done.

Min. Value:	000
Max. Value:	010

Recommended Value: 000

TXTV
Change TXTV by pressing Left/Right buttons to adjust the proper vertical size of Teletext screen. Check and readjust TRPEZ item if the adjustment becomes improper after some other geometric adjustments are done.

Min. Value: 000
Max. Value: 040
Recommended Value: 015

16.3.VIDEO ALIGNMENTS
Switch the program to colour bar test pattern. Press GREEN button to access this group of item. Select the parameter by pressing up/down buttons. Adjust the parameter by pressing left/right buttons. Store the settings by pressing OK button.

WdR, WdG, WdB: WHITE BALANCE ADJUSTMENT
Apply WHITE test pattern via RF. Adjust all analog functions to medium level and set WdR to 86, WdG to 84, WdB to 80, if needed. Use colour analyser and monitor the colour temperature (X,Y) on colour analyser. Select WdR and WdB by pressing up/down buttons and change the values by Left/Right buttons till the following values are read:
X=285±10
Y=293±10 on the colour analyser.

CuR, CuG, CuB
Set the values of these items as 64 (constant).

YDFP
Enter a PAL B/G colour and black-white bar test pattern via RF. Adjust Y-Delay for PAL till the colour transients on the colour bar of the pattern become as sharper and colours between transients do not mix with each other as possible.

Min. Value: -07
Max. Value: 001
Recommended Value: -05

AGC
Apply PAL BG signal, VHF-3 Channel-12 and 60dBmV signal level. Adjust AGC (Automatic Gain Control) item by pressing Left/Right buttons till the voltage at AGC point (pin1 of the tuner) becomes 3.0 volts.

Min. Value: 000
Max. Value: 015
Recommended Value: 009

TLAN
Text language is set. Options are W-T, W-E, W, E. W-T will be selected.

APS
The option of APS (Automatic Program Searching) item are ON and OFF. In order to active APS installation procedure when TV is turned for the very first time, select ON. Inorder to start TV without APS installation procedure, select OFF.

T_T
This item is used for the Tuner selection. The options are SAM for SAMSUNG, THO for THOMSON, SIE for SIEMENS, MK2 and MK3 for PHILIPS MP2/MP3, ALP for ALPS and TEC for Tecnisat. Select THO.

T_P
This item is also used for the Tuner selection. The options are MK2, SAM, THO, TEM. MK2 for PHILIPS, SAM for SAMSUNG, THO for THOMSON and TEM for TEMIC. Select SAM.

YDFS
Enter a SECAM B/G colour and black-white bar test pattern via RF. Adjust Y-Delay SECAM till the colour transients on the colour bar of the pattern become as sharper and colours between transients do not mix with each other as possible.

Min. Value:	-07
Max. Value:	001
Recommended Value:	-07

YDFN
Enter an NTSC colour and black-white bar test pattern via RF. Adjust Y-Delay NTSC till the colour transients on the colour bar of the pattern become as sharper and colours between transients do not mix with each other as possible.

Min. Value:	-07
Max. Value:	001
Recommended Value:	-02

EXT3
Select ON.

DVD
Select OFF.

C.M
Select ON.

BLUE
Select OFF.

4:3
Set to 0.

OVM
Select ON.

16.4.SERVICE ALIGNMENTS

IMPORTANT: There will no adjustments in this service mode during production mode alignments.
Press BLUE colour button on the remote control when Production mode is active. Press the colour button of the related item group headline colour. Press up/down buttons to select the item of group. Press Left/Right button to alter the value of the item. Press OK button to store the selected value and MENU button to exit the service alignments mode.

ADJUSTMENTS GROUP
Press RED button in order to access this group of items.

PIP CNTRST	: Level of the PIP picture
PIP Ydelay	: Luma delay of the PIP picture
PIP Frame	: Colour selection of the PIP frame (edges of the PIP)
EHTHP	: EHT compensation coefficient for horizontal phase
EHTH TC	: EHT time constant for horizontal phase compensation
EHTH	: EHT compensation coefficient for horizontal amplitude
EHTV	: EHT compensation coefficient for vertical amplitude
EHTV TC	: EHT time constant for control of vertical and horizontal amplitude EHT compensation
SVDEL	: Delay adjustment for scan velocity modulation
BCLTHR (mA)	: Beam current applied to the CRT
OSD CONT	: Contrast level of OSD
OSD BRI	: Brightness level of OSD
TEXT BRI	: Brightness level of text
PIP YDelSe	: Y-Delay adjustment for pin-in-picture option
INIT NVM	: Press to initiate the NVM

PRESCALER GROUP

Press GREEN button in order to access this group of items.

FM : This adjustment is to determine the pre-amplifier gain of MSP for German stereo
Set to 27.

NICAM : This adjustment is to determine the pre-amplifier gain of MSP for Nicam
Set to 61.

I2S : Not used.

SCART : This adjustment is to determine the pre-amplifier gain of MSP for Scart audio inputs
Set to 25.

OPTIONS GROUP

Press BLUE button in order to access this group of items.

0.HPHONE : ON/OFF
1.CRT : 4:3 / 16:9
2.SVHS : ON/OFF
3.f(IF) : always set to 38.9
4.Türk. : Turkish menu ON/OFF
5.VGA : ON/OFF
6.FRONT : Front AV ON/OFF
7.DPL : ON/OFF
8.VD : ON/OFF
9.NSL : ON/OFF
A.PAP : ON/OFF
B.CTI : ON/OFF
C.AVL : ON/OFF

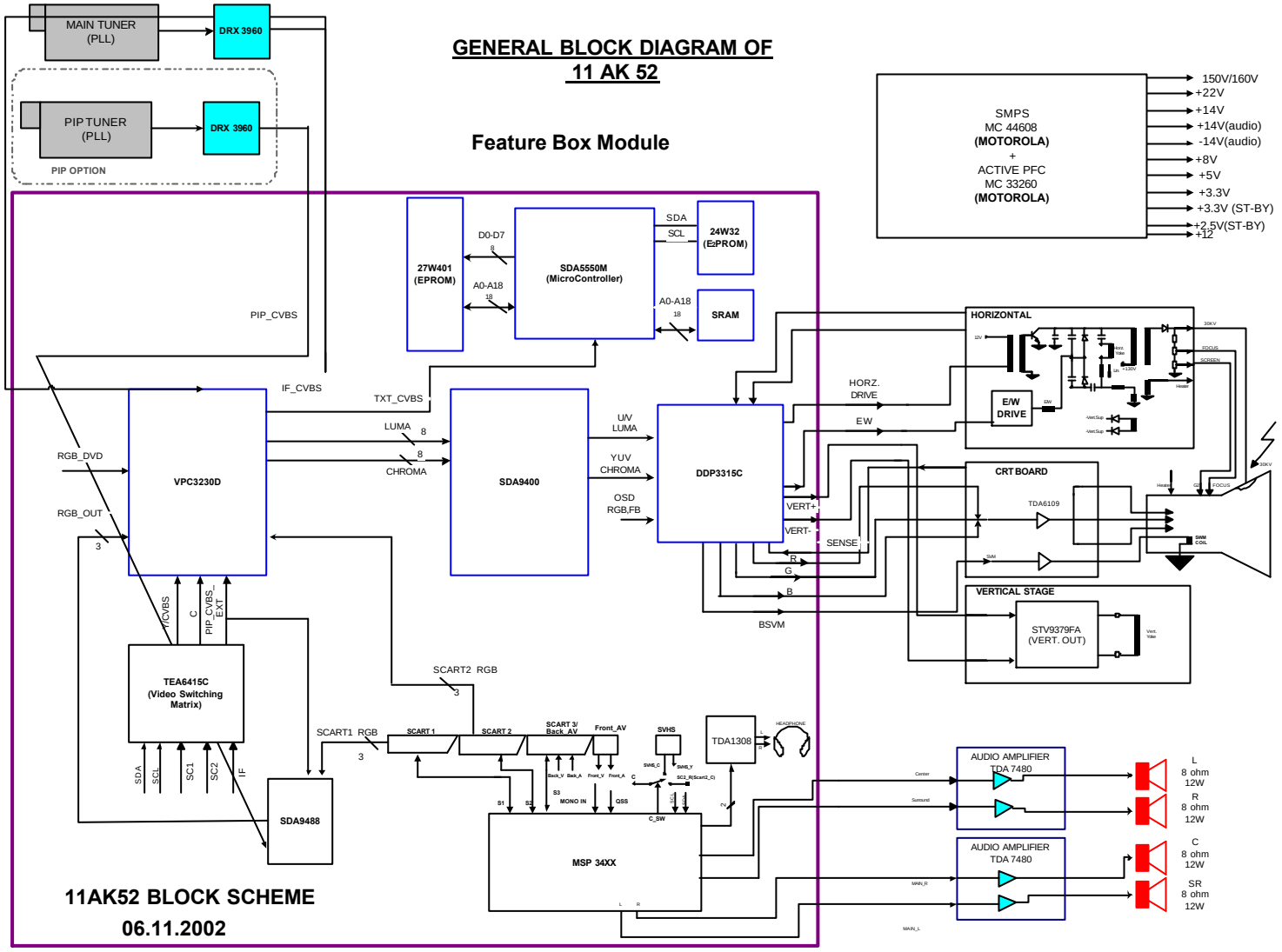
SYSTEM GROUP

Press YELLOW button in order to access this group of items.

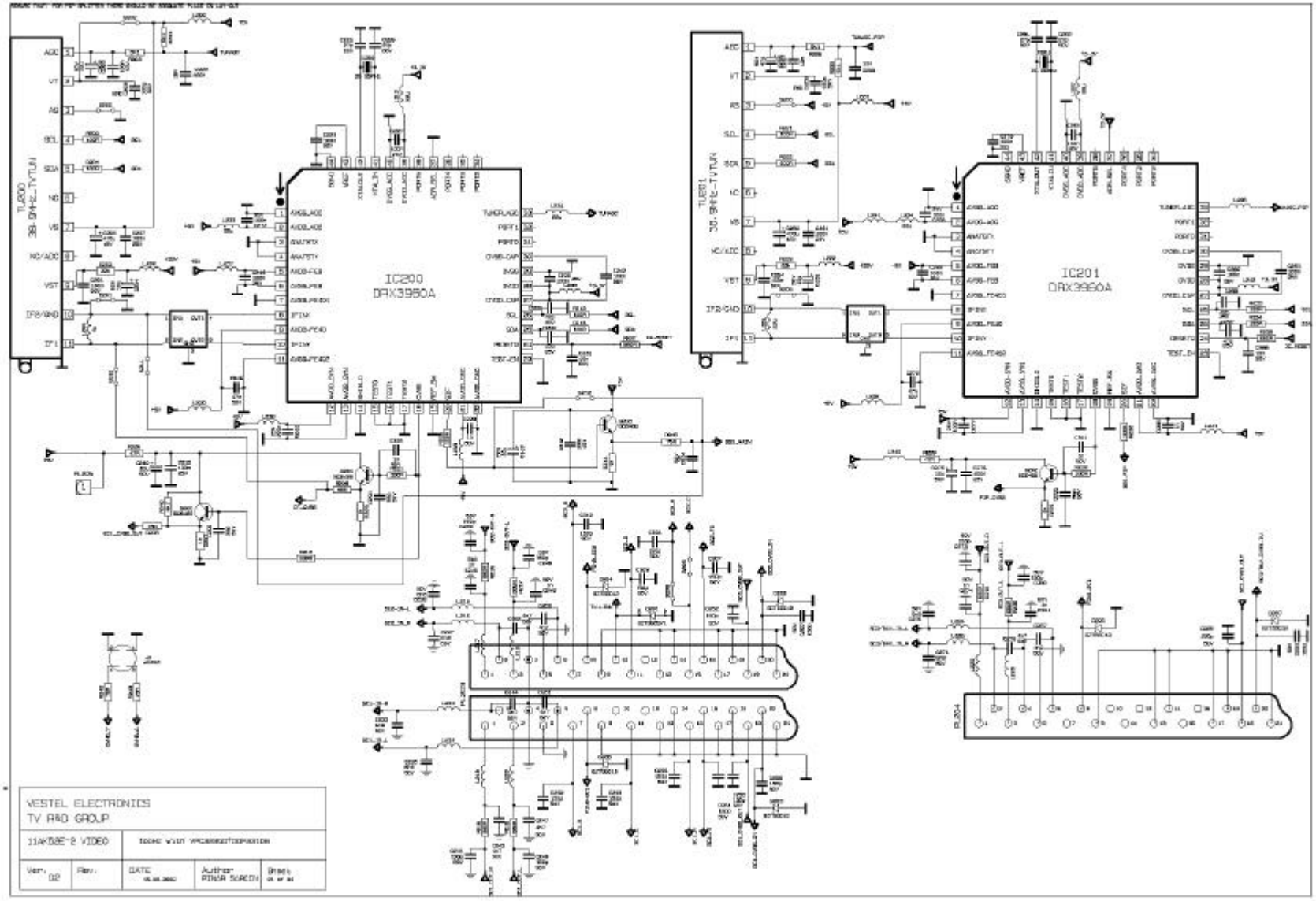
0.PAL B/G : ON/OFF
1.PAL D/K : ON/OFF
2.PAL I : ON/OFF
3.SECAM B/G : ON/OFF
4.SECAM D/K : ON/OFF
5.SECAM L/L' : ON/OFF
6.AUST. : ON/OFF

NOTE: Settings values in Service menu are given for 28" 4:3 THOMSON (A66EHJ13X12) tube in this manual.

17.BLOCK DIAGRAM



18.CIRCUIT DIAGRAMS



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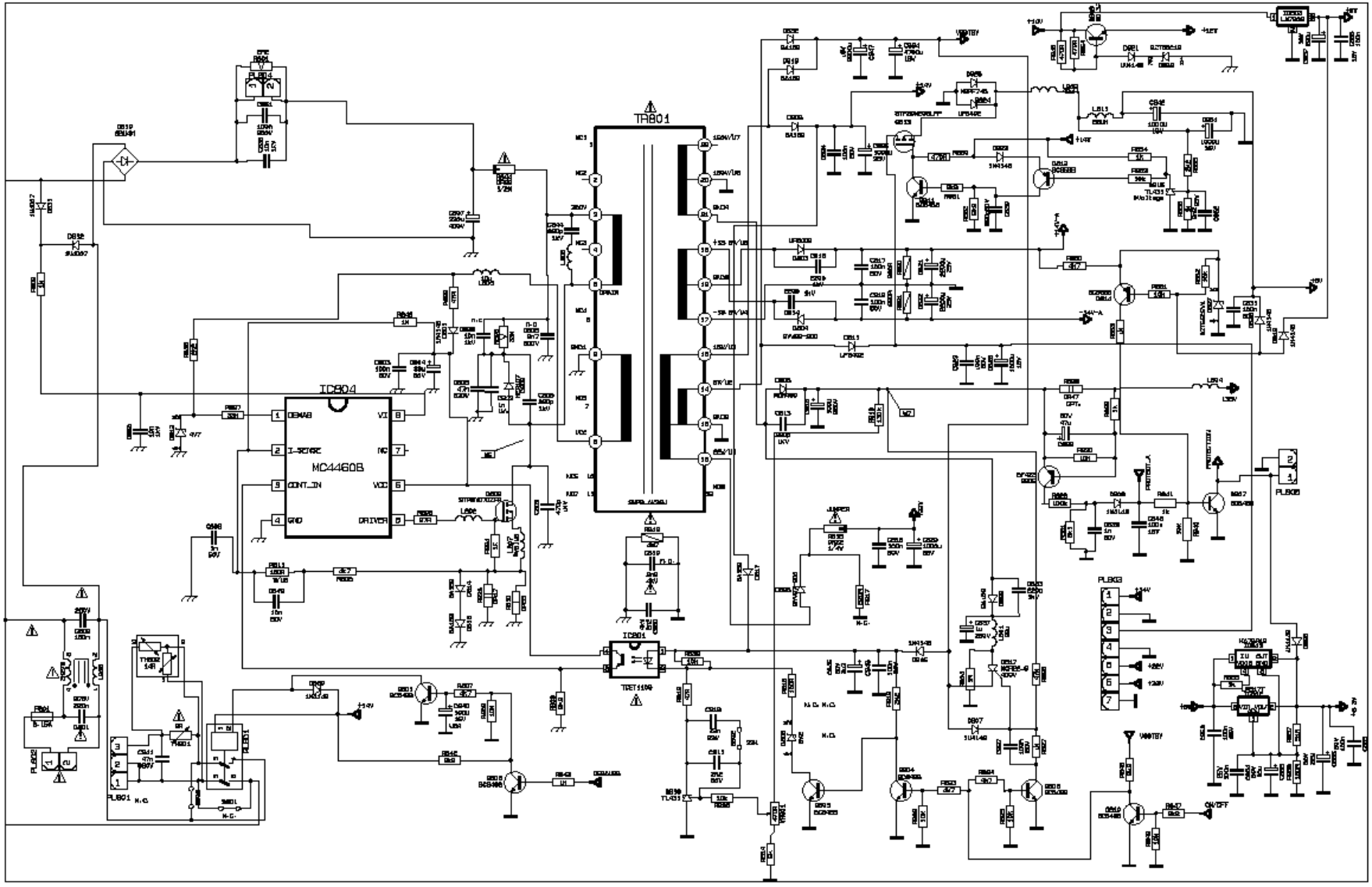
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MC44608
DEMAG
I-SENSE
CONT_IN
GND
VCC
DRIVER
IC801
TL431

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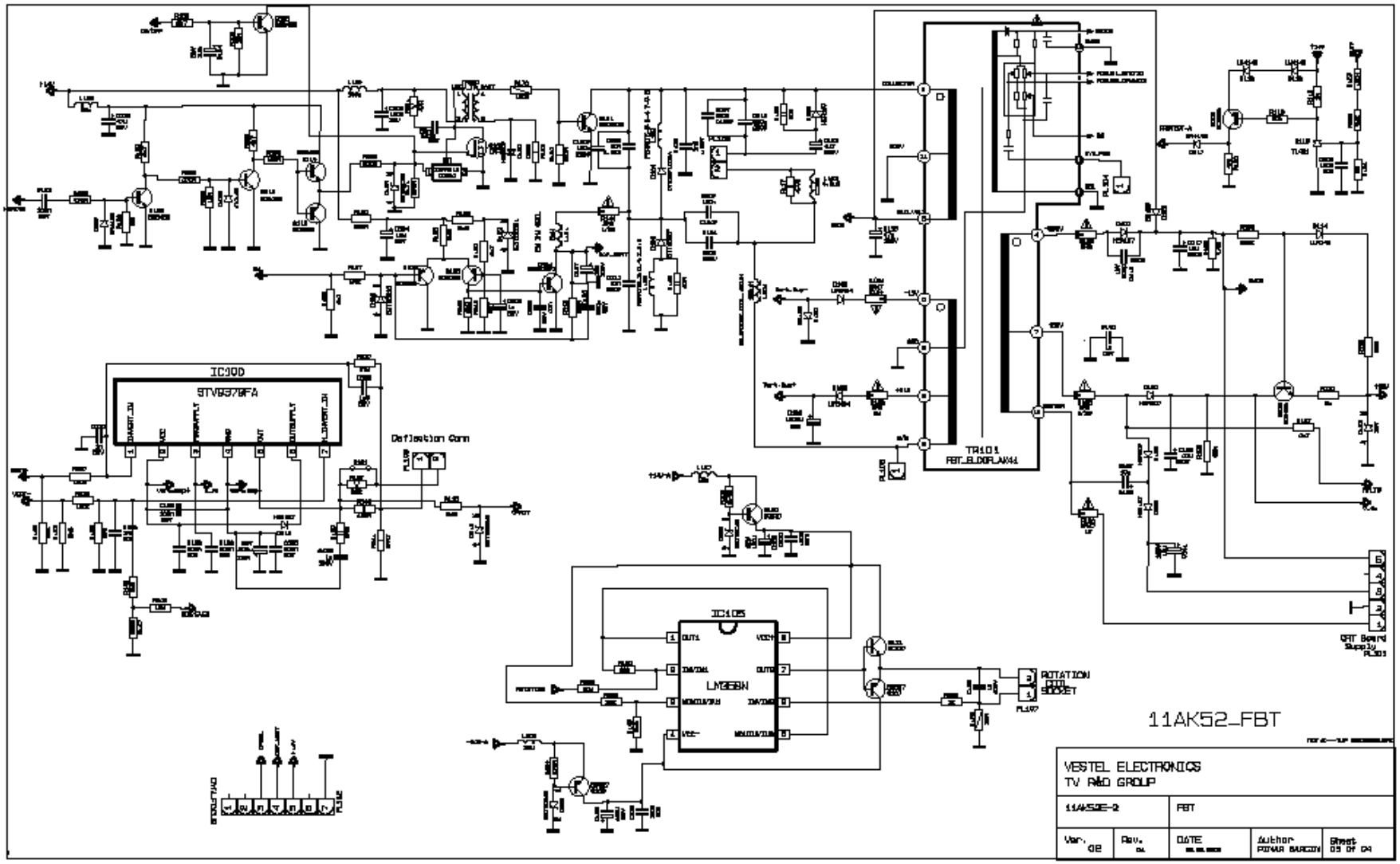
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STV8978FA
Deflection Conn
TR101
FBT_BLOOPLAN44
IC105
LM2588N
ROTATION
COIL
SOCKET
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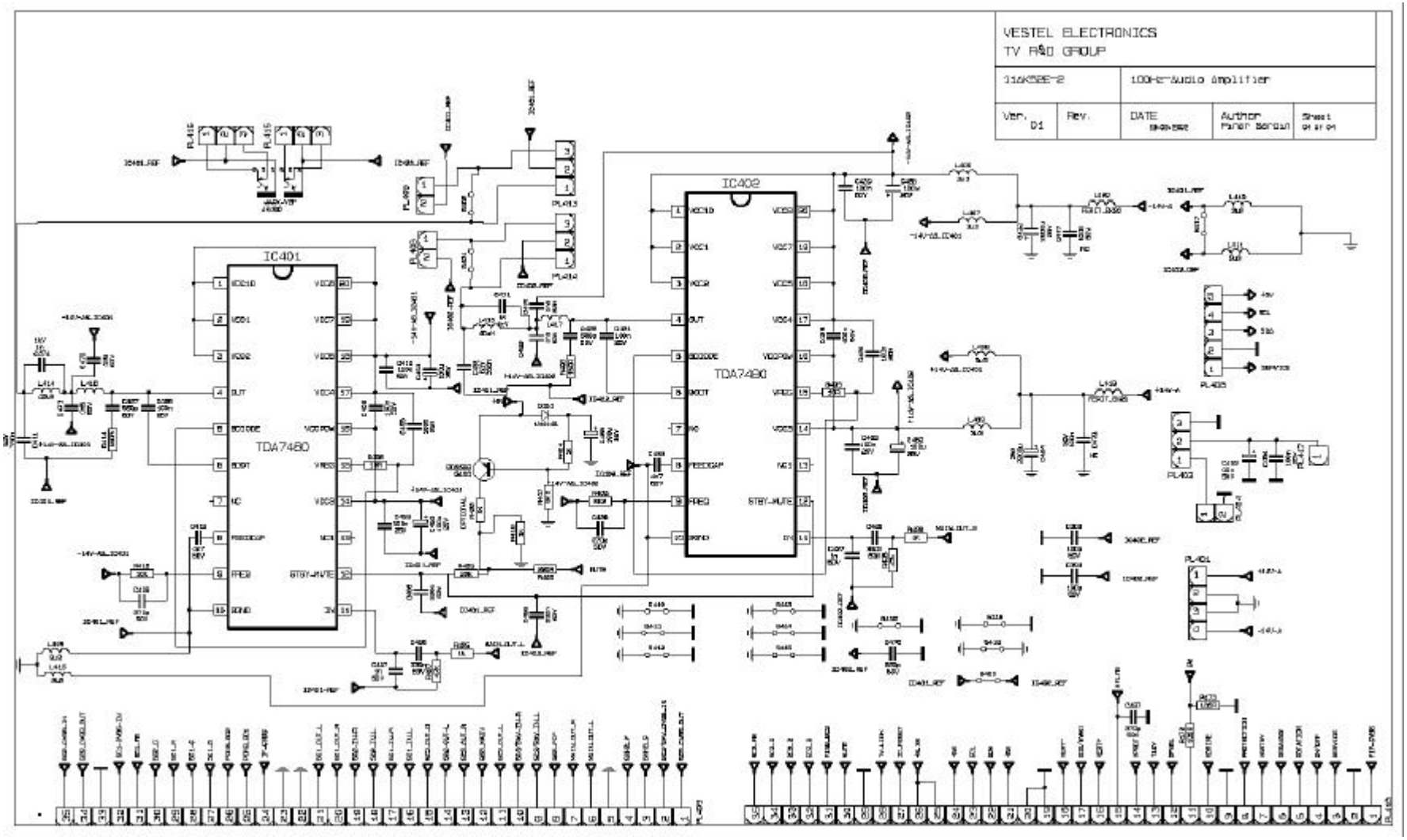
VESTEL ELECTRONICS
TV R&D GROUP
11AK52E-2
FBT
Ver.
02
Rev.
01
DATE
Author
POYRAZ BARCIN
Sheet
03 OF 04

11ak52e3-3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TV R&D GROUP
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Rev.
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Author
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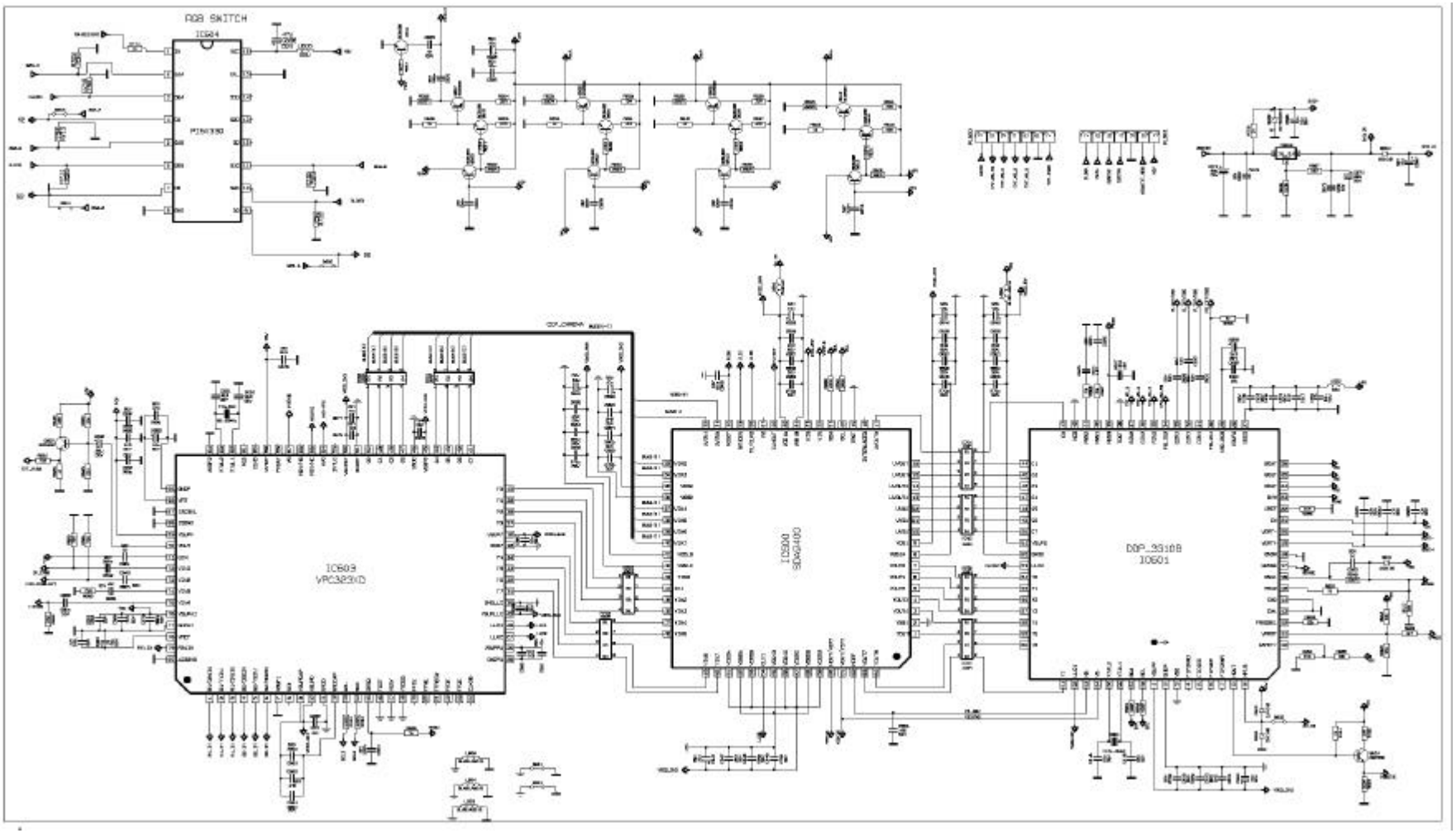
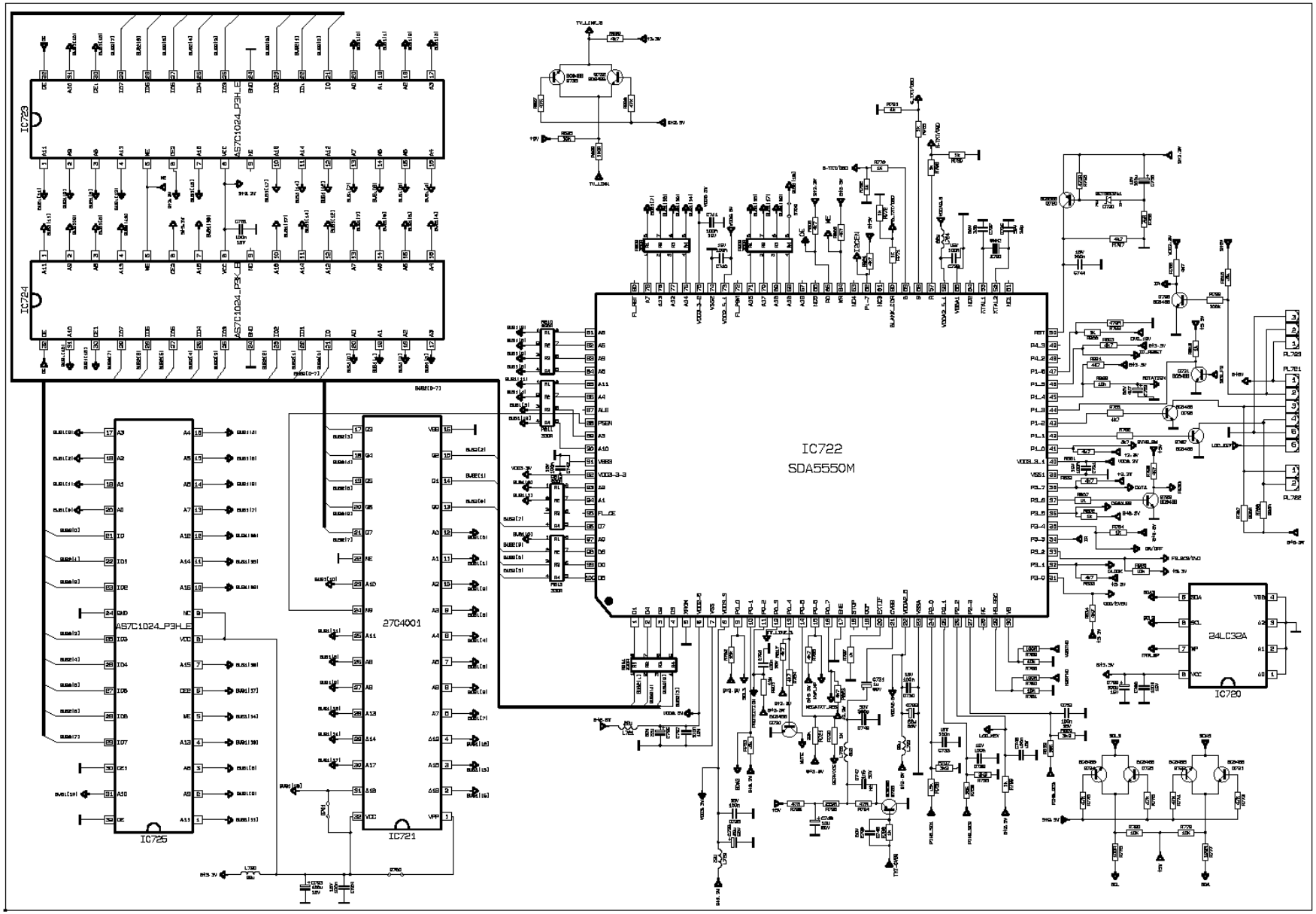
IC401
TDA7480
IC402
TDA7480

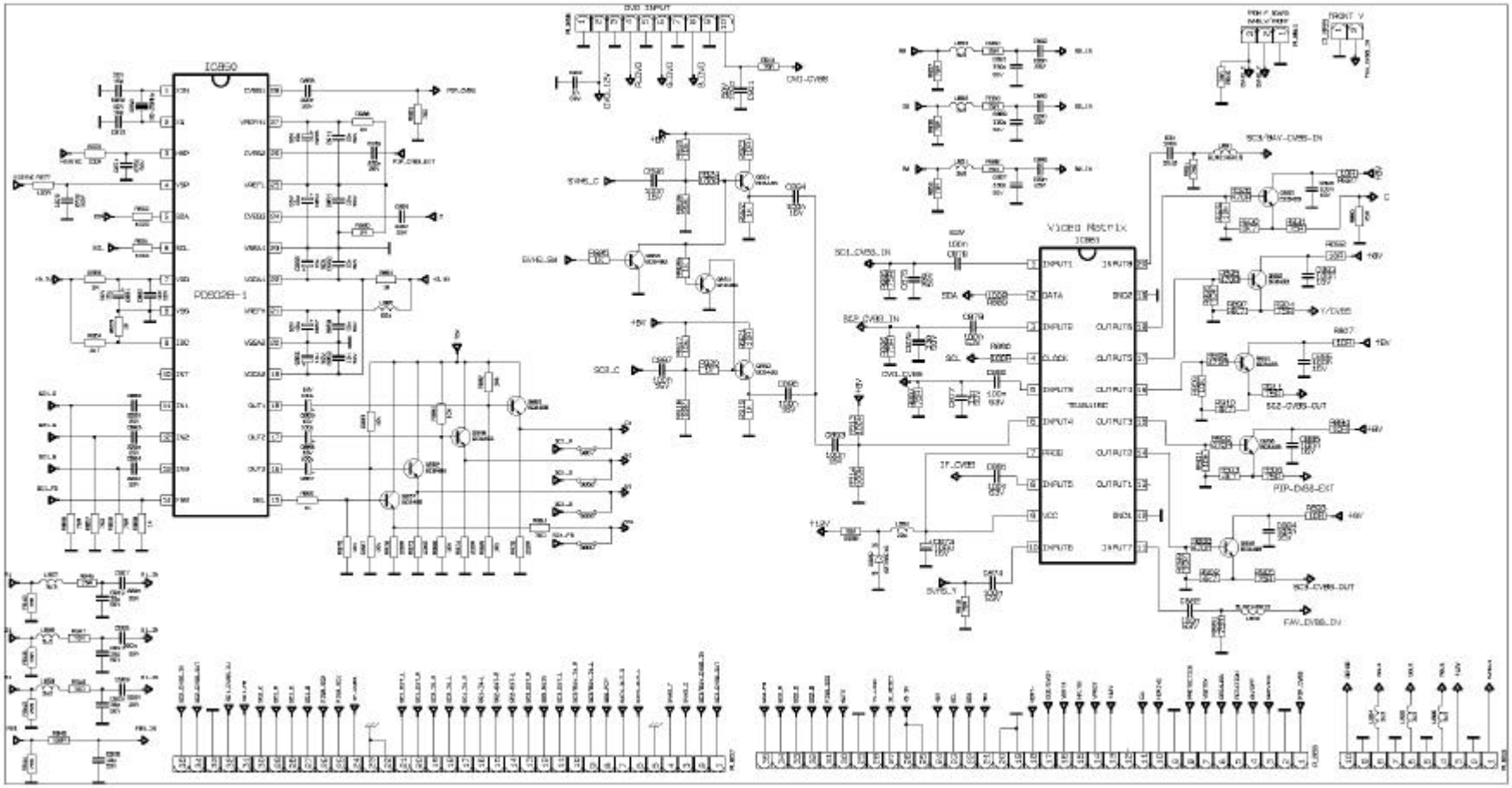
11ak52e3-4


RGB SWITCH
IC604
IC603
VPC3230D
IC500
SDA9403
DDP_3310B
IC601

11fb2a1—1


IC722
SDA5550M
IC723
IC724
IC725
IC721
IC720
AS7C1024_P3H_LE
27C4001
24LC32A

11fb2a1—2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Video Matrix
IC853
DVD INPUT
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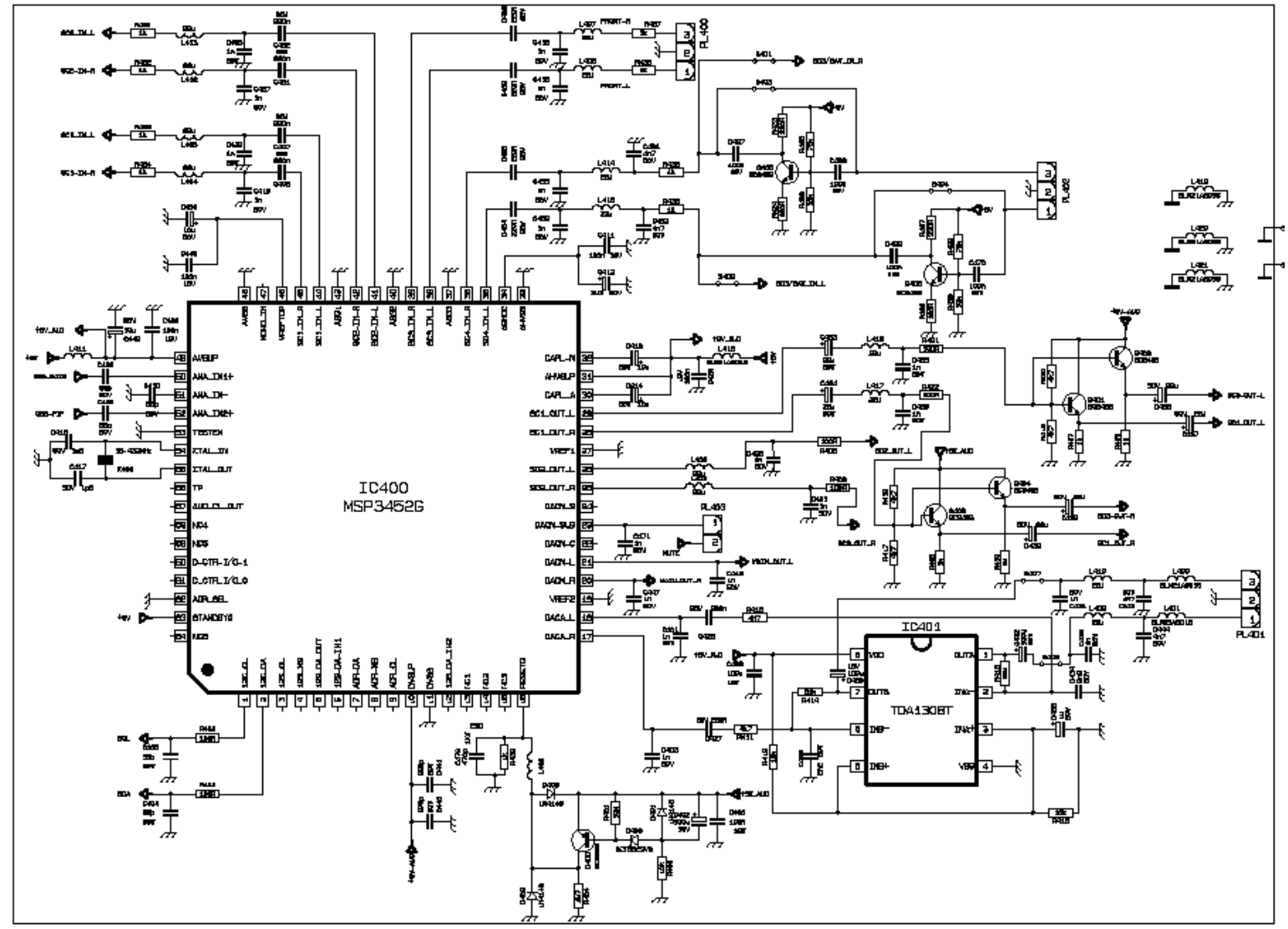
SDA_CVBS_IN
SCL
SDA
SCL_C
SDA_C
5V
12V
+5V
+12V
Y/CVBS
SCART-CVBS-OUT
PIP-CVBS-EXT
SCART-CVBS-OUT
FAV_CVBS_OUT
FRONT V

11fb2a1—3



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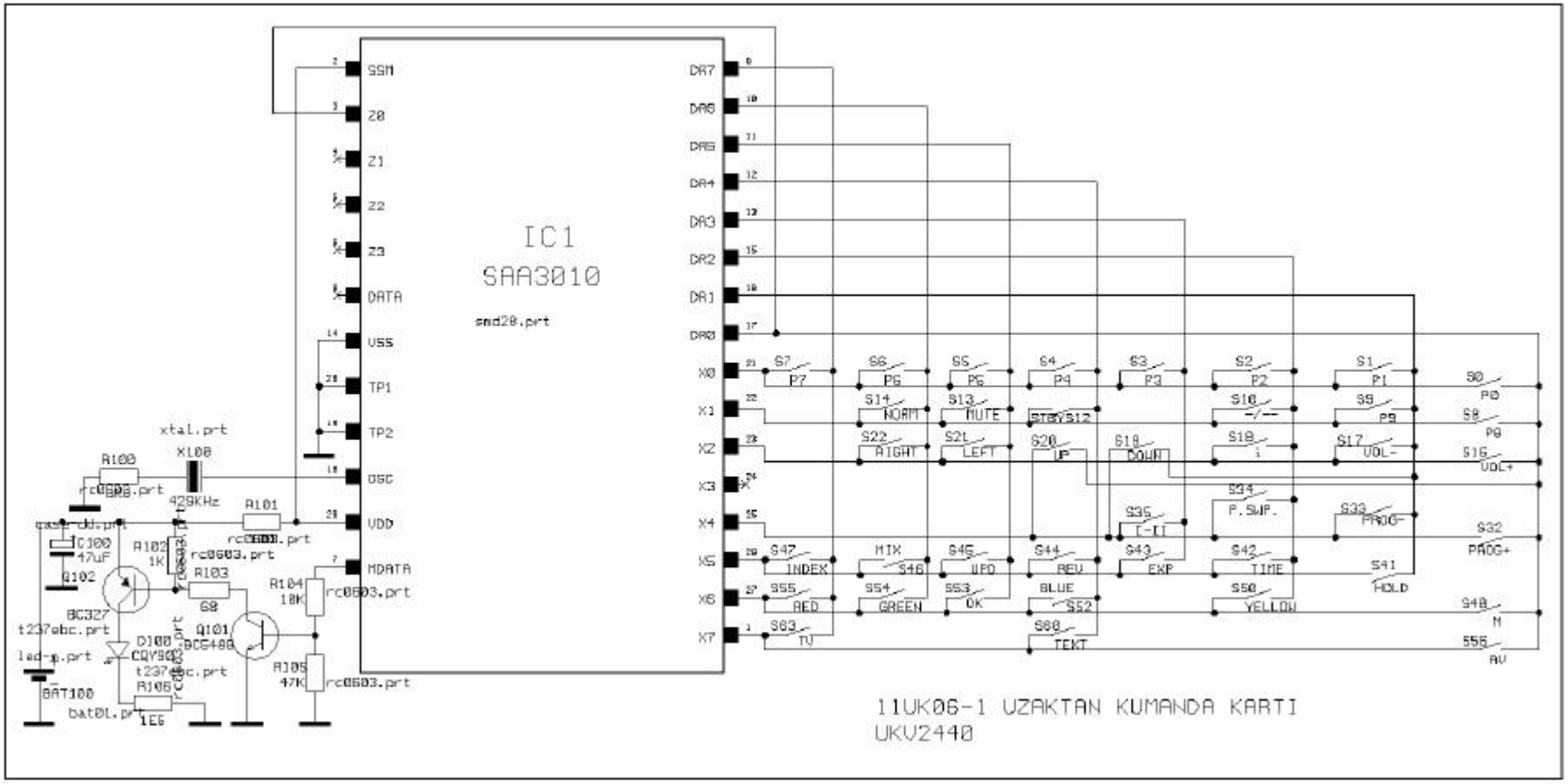
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SAA3010
smd28.prt
SSM
Z0
Z1
Z2
Z3
DATA
VSS
TP1
TP2
OSC
VDD
MDATA
DR7
DR6
DR5
DR4
DR3
DR2
DR1
DR0
X0
X1
X2
X3
X4
X5
X6
X7
xtal.prt
X100
429KHz
R100
R101
C100
47uF
Q102
R102
1K
R103
68
R104
18K
R105
47K
R106
1E6
Q101
BC548
D100
CQY90
BC327
t237abc.prt
led-p.prt
BAT100
bat0L.prt
S7 P7
S6 P6
S5 P5
S4 P4
S3 P3
S2 P2
S1 P1
S0 P0
S14 NORM
S13 MUTE
S12
S10 -/--
S9 P9
S8 P8
S22 RIGHT
S21 LEFT
S20 UP
S19 DOWN
S18
S17 VOL-
S16 VOL+
S34 P.SWP.
S33 PROG-
S32 PROG+
S35 [-II
S47 INDEX
S46 MIX
S45 UPD
S44 REV
S43 EXP
S42 TIME
S41 HOLD
S55 RED
S54 GREEN
S53 OK
S52 BLUE
S50 YELLOW
S49 M
S48
S03 TV
S00 TEXT
555 AV
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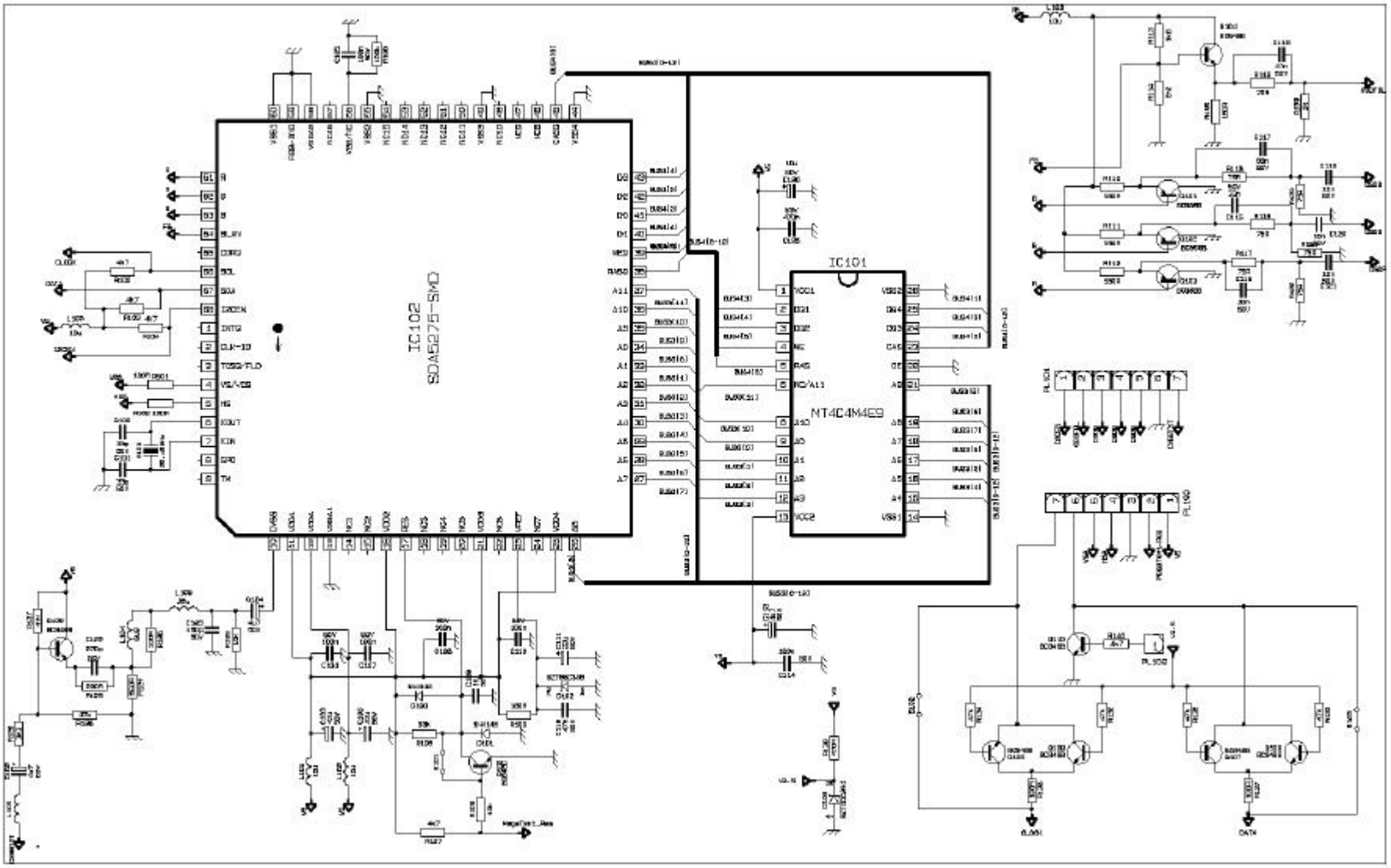
UKU2440

11uk06-1



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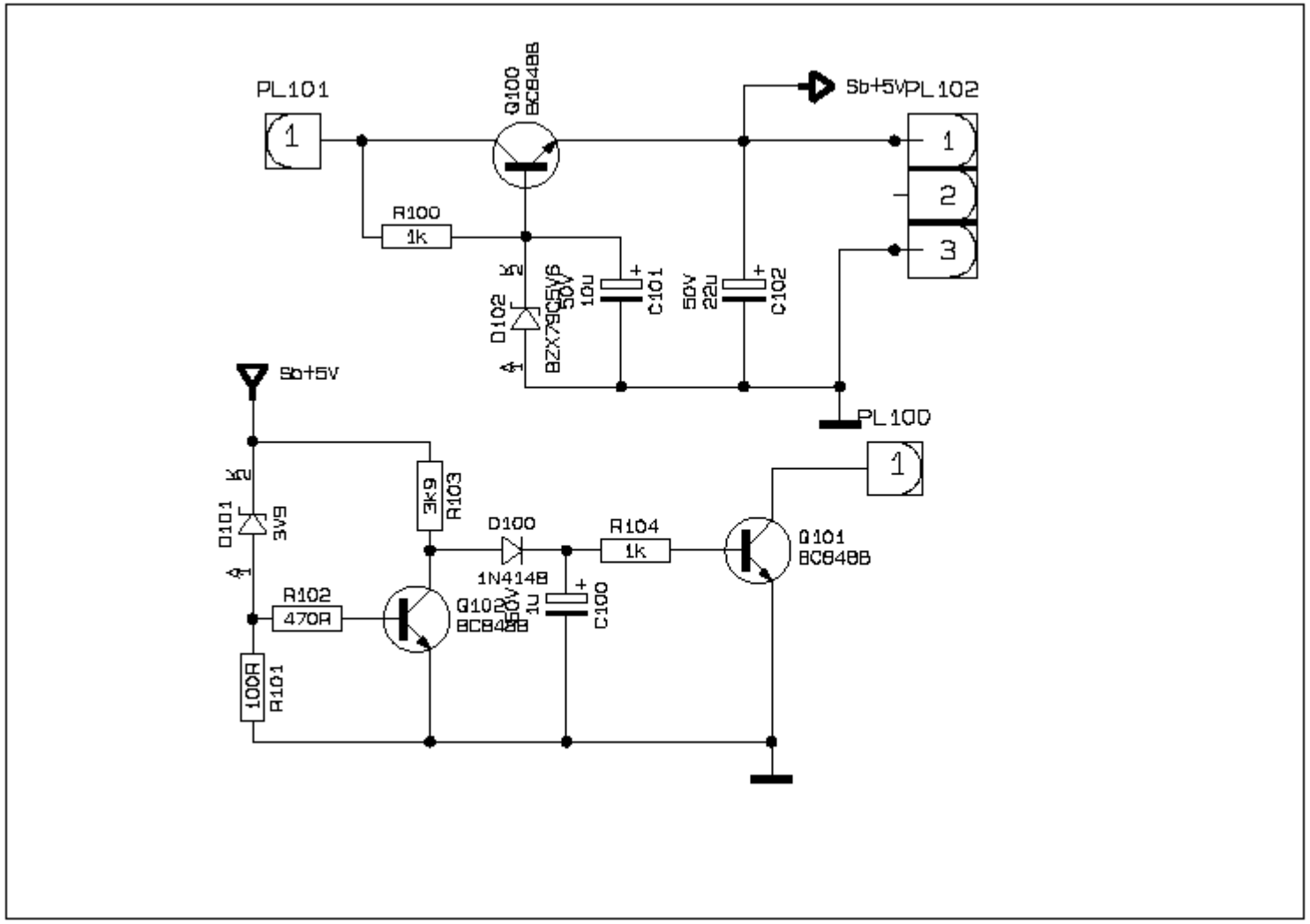
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1
Q100
BC848B
Sb+5V
PL102
1
2
3
R100
1k
D102
BZX79C5V6
50V
10u
C101
50V
22u
C102
Sb+5V
PL100
1
D101
3V9
3k9
R103
D100
1N414B
R104
1k
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BC848B
R102
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Q102
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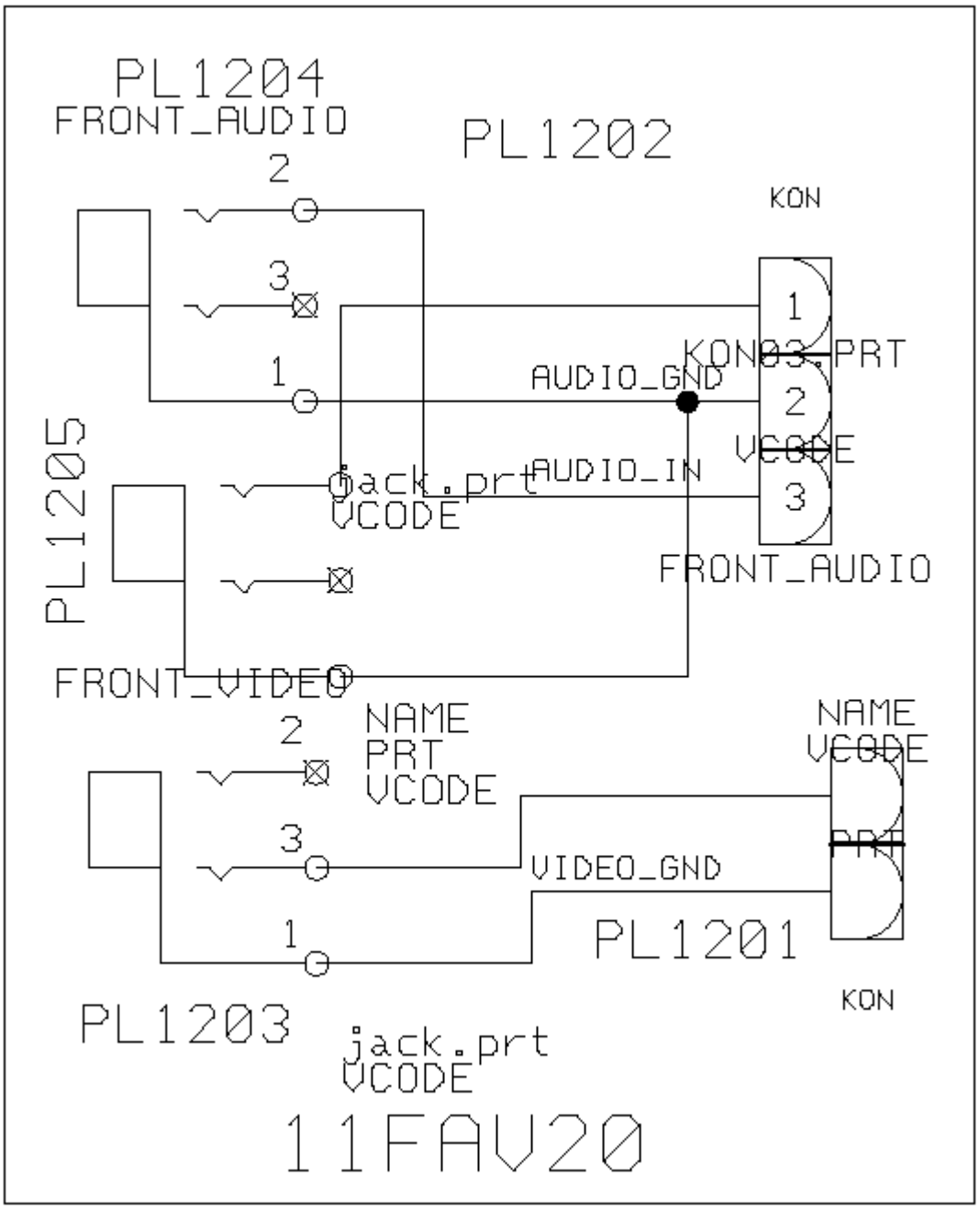
1u
C100
100R
R101

11rs52


PL1204
FRONT_AUDIO
PL1202
KON
2
3
1
1
KON03.PRT
AUDIO_GND
2
VCODE
AUDIO_IN
3
jack.prt
VCODE
PL1205
FRONT_AUDIO
FRONT_VIDEO
2
NAME
PRT
VCODE
NAME
VCODE
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PRT
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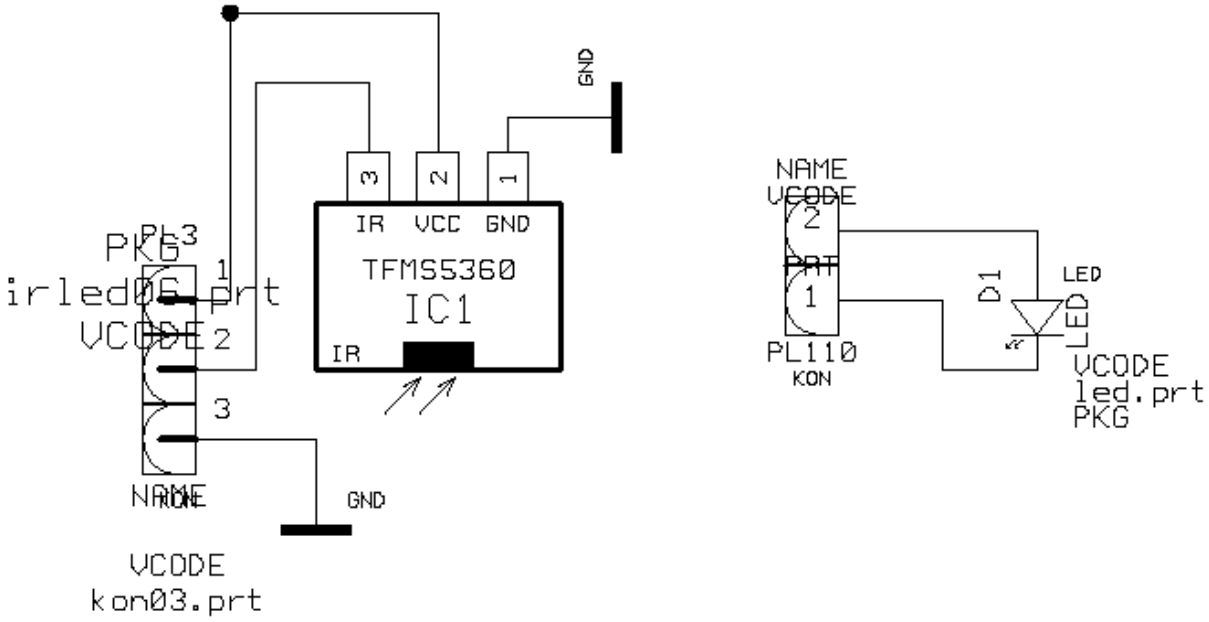
PL1203
jack.prt
VCODE
11FAV20

11fav19a4



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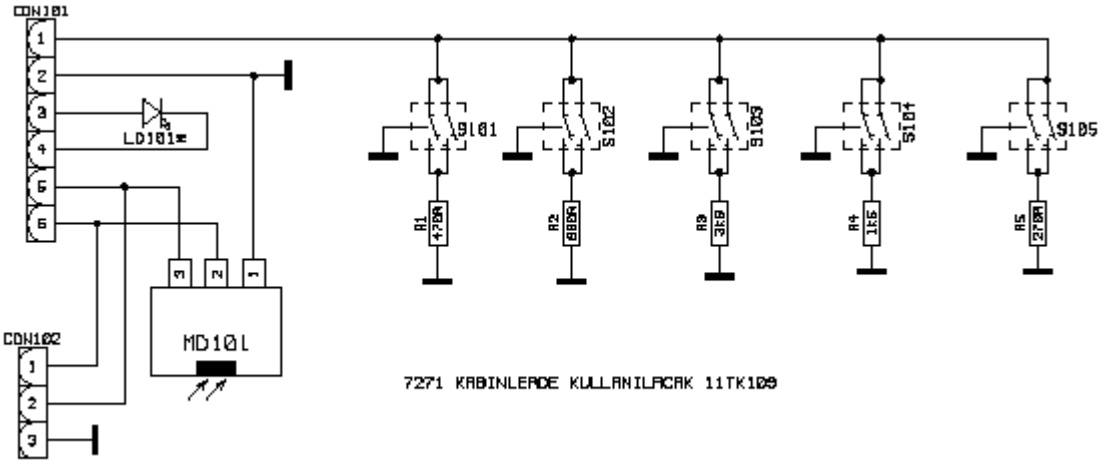

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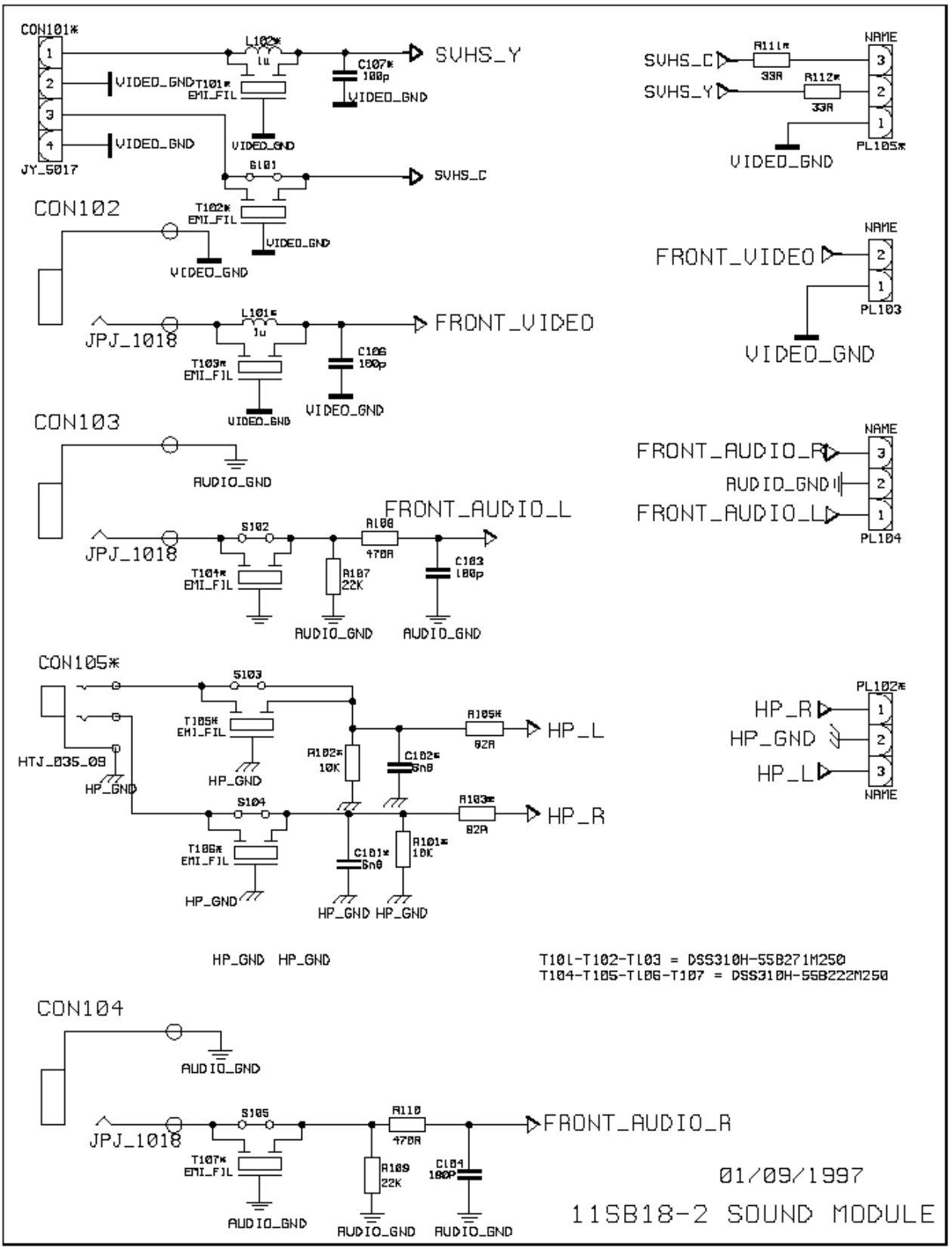
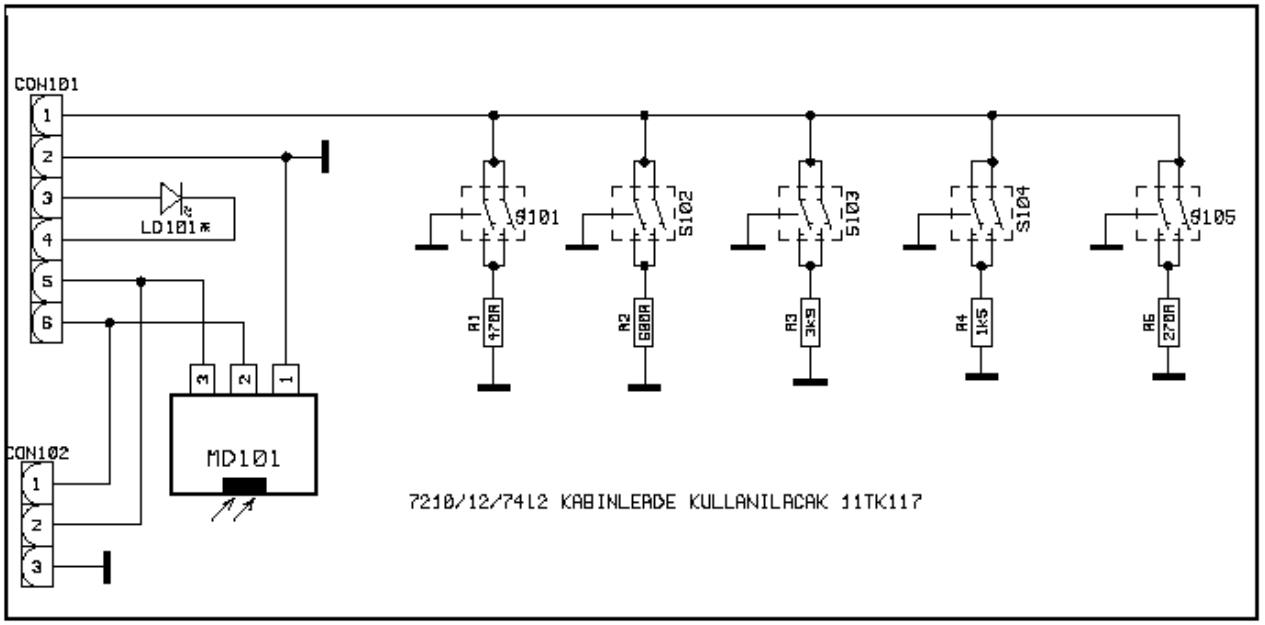
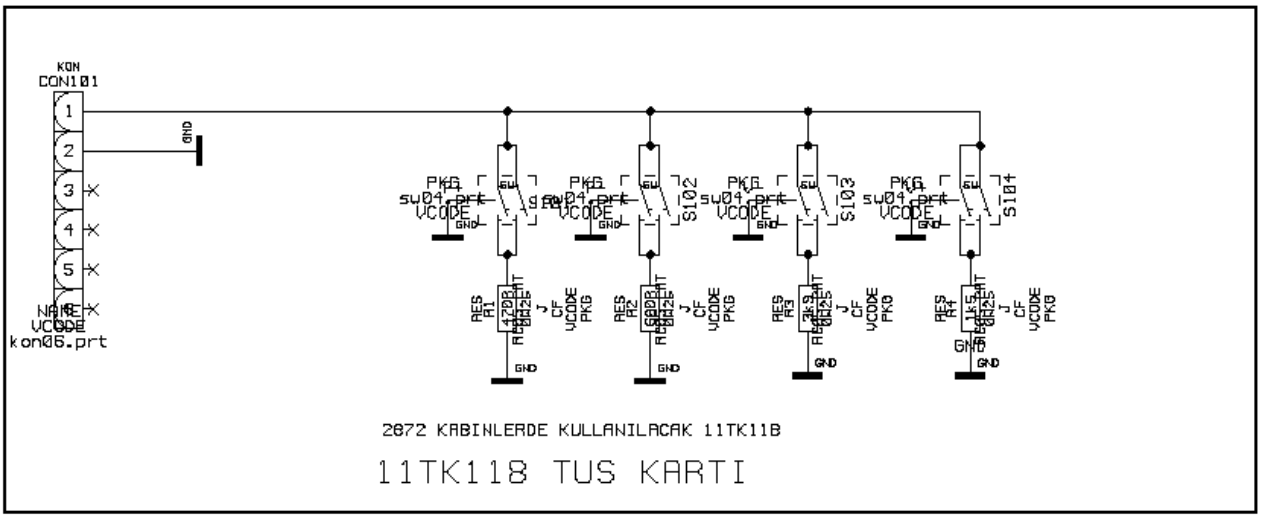

CON101*
JY_5017
L102*
1u
C107*
100p
SVHS_Y
VIDEO_GND
T101*
EMI_FIL
VIDEO_GND
VIDEO_GND
G101
SVHS_C
CON102
T102*
EMI_FIL
VIDEO_GND
VIDEO_GND
JPJ_1018
L101*
1u
FRONT_VIDEO
T103*
EMI_FIL
C106
100p
VIDEO_GND
VIDEO_GND
CON103
AUDIO_GND
FRONT_AUDIO_L
JPJ_1018
S102
R108
470R
T104*
EMI_FIL
R107
22K
C103
100p
AUDIO_GND
AUDIO_GND
CON105*
S103
T105*
EMI_FIL
R105*
82R
HP_L
HTJ_035_09
HP_GND
R102*
10K
C102*
5n6
S104
R103*
82R
HP_R
T106*
EMI_FIL
C101*
5n6
R101*
10K
HP_GND
HP_GND
HP_GND
HP_GND HP_GND
T101-T102-T103 = DSS310H-55B271M250
T104-T105-T106-T107 = DSS310H-55B222M250
CON104
AUDIO_GND
JPJ_1018
S105
R110
470R
FRONT_AUDIO_R
T107*
EMI_FIL
R109
22K
C104
100P
AUDIO_GND
AUDIO_GND
AUDIO_GND
01/09/1997
11SB18-2 SOUND MODULE
SVHS_C
SVHS_Y
R111*
33R
R112*
33R
NAME
PL105*
VIDEO_GND
FRONT_VIDEO
NAME
PL103
VIDEO_GND
FRONT_AUDIO_R
AUDIO_GND
FRONT_AUDIO_L
NAME
PL104
PL102*
HP_R
HP_GND
HP_L
NAME

11sb18-3



11tk117



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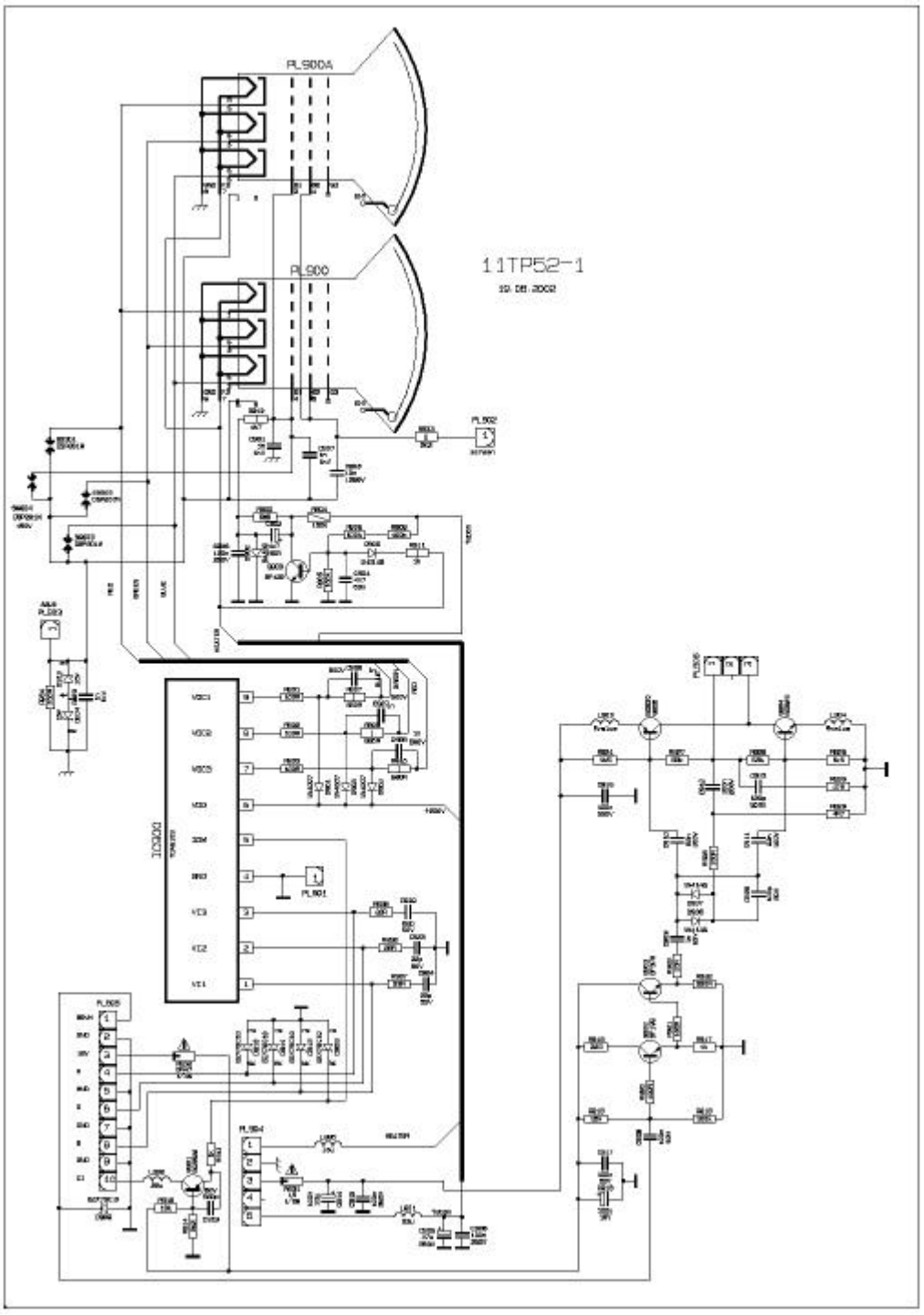
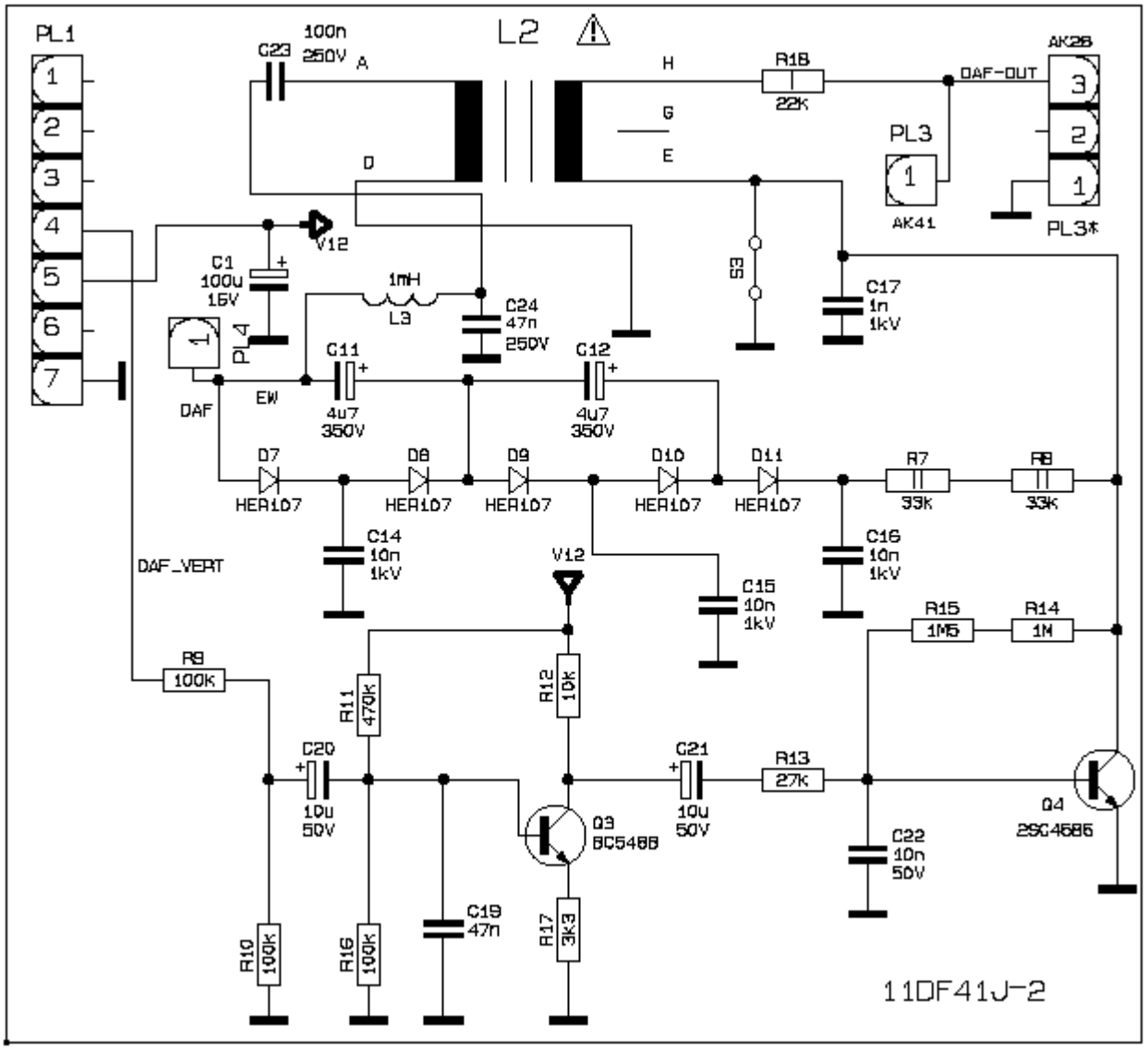


11tp52-1


PL1
C23 100n 250V
L2
A
H
R18 22K
DAF-OUT
AK26
PL3
AK41
PL3*
G
E
D
V12
C1 100u 16V
1mH
L3
C24 47n 250V
PL4
C11 4u7 350V
C12 4u7 350V
S3
C17 1n 1kV
DAF
EW
D7 HER107
D8 HER107
D9 HER107
D10 HER107
D11 HER107
R7 33K
R8 33K
C14 10n 1kV
C16 10n 1kV
C15 10n 1kV
DAF_VERT
R15 1M5
R14 1M
R9 100K
R11 470K
R12 10K
C20 10u 50V
C21 10u 50V
R13 27K
Q3 BC548B
Q4 2SC4686
C22 10n 50V
C19 47n
R17 3K3
R10 100K
R16 100K
11DF41J-2

11df41j-2

SM52-PHILIPS_IF

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1.INTRODUCTION

11AK52 is a 100Hz flicker free colour television capable of driving 28”4:3/16:9, 32” 16:9, 33”4:3 and 29”4:3 real flat picture tubes.
The chassis is capable of operation in PAL, SECAM, NTSC (playback) colour standards and multiple transmission standards as B/G, D/K, I/I’, and L/L´.
Sound system output is supplying 2x10W (10%THD) for left and right outputs of 8ohm speakers.
TV supports the level 1.5 teletext standard. It is possible to decode transmissions including high graphical data.
The chassis is equipped with two full EuroScarts, one SCART for AV input/output, one front-AV input, one back-AV input, one headphone output, one SVHS input (via SCART and SVHS connector), two external speaker outputs (left and right).

2.TUNER

The hardware and software of the TV is suitable for tuners, supplied by different companies, which are selected from the Service Menu. These tuners can be combined VHF, UHF tuners suitable for CCIR systems B/G, H, L, L´, I/I´, and D/K. The tuning is available through the digitally controlled I²C bus (PLL). Below you will find info on one of the Tuners in use.

General description of UV1316:
The UV1316 tuner belongs to the UV 1300 family of tuners, which are designed to meet a wide range of applications. It is a combined VHF, UHF tuner suitable for CCIR systems B/G, H, L, L’, I and I’. The low IF output impedance has been designed for direct drive of a wide variety of SAW filters with sufficient suppression of triple transient.

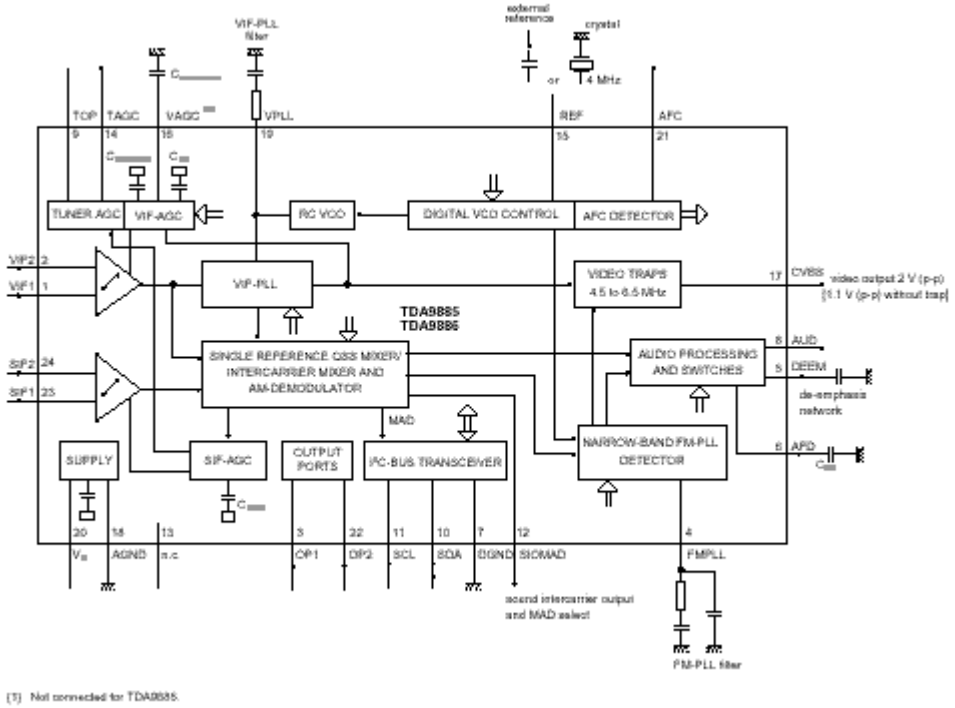
Features of UV1316:
1. Member of the UV1300 family small sized UHF/VHF tuners
2. Systems CCIR: B/G, H, L, L’, I and I’; OIRT: D/K
3. Digitally controlled (PLL) tuning via I²C-bus
4. Off-air channels, S-cable channels and Hyperband
5. World standardized mechanical dimensions and world standard pinning
6. Compact size
7. Complies to “CENELEC EN55020” and “EN55013”

Pinning:

1.	Gain control voltage (AGC)	:	4.0V, Max: 4.5V
2.	Tuning voltage		
3.	I²C-bus address select	:	Max: 5.5V
4.	I²C-bus serial clock	:	Min:-0.3V, Max: 5.5V
5.	I²C-bus serial data	:	Min:-0.3V, Max: 5.5V
6.	Not connected		
7.	PLL supply voltage	:	5.0V, Min: 4.75V, Max: 5.5V
8.	ADC input		
9.	Tuner supply voltage	:	33V, Min: 30V, Max: 35V
10.	Symmetrical IF output 1		
11.	Symmetrical IF output 2		

3.IF PART (TDA9885/86)

The TDA9885 is an alignment-free single standard (without positive modulation, only PAL) vision and sound IF signal PLL.
The TDA9886 is an alignment-free multistandard (PAL, SECAM and NTSC) vision and sound IF signal PLL Both devices can be used for TV, VTR, PC and set-top box applications.
The following figure shows the simplified block diagram of the integrated circuit.
The integrated circuit comprises the following functional blocks:
VIF amplifier, Tuner and VIF-AGC, VIF-AGC detector, Frequency Phase-Locked Loop (FPLL) detector, VCO and divider, Digital acquisition help and AFC, Video demodulator and amplifier, Sound carrier trap, SIF amplifier, SIF-AGC detector, Single reference QSS mixer, AM demodulator, FM demodulator and acquisition help, Audio amplifier and mute time constant, I²C-bus transceivers and MAD (module address), Internal voltage stabilizer.



4.VIDEO SWITCH TEA6415

In case of three or more external sources are used, the video switch IC TEA6415 is used. The main function of this device is to switch 8 video-input sources on the 6 outputs.

Each output can be switched on only one of each input. On each input an alignment of the lowest level of the signal is made (bottom of sync. top for CVBS or black level for RGB signals).

Each nominal gain between any input and output is 6.5dB.For D2MAC or Chroma signal the alignment is switched off by forcing, with an external resistor bridge, 5VDC on the input. Each input can be used as a normal input or as a MAC or Chroma input (with external Resistor Bridge). All the switching possibilities are changed through the BUS. Driving 75ohm load needs an external resistor. It is possible to have the same input connected to several outputs.

5.MULTI STANDARD SOUND PROCESSOR

The MSP34x1G family of single-chip Multi-standard Sound Processors covers the sound processing of all analog TV-Standards worldwide, as well as the NICAM digital sound standards. The full TV sound processing, starting with analog sound IF signal-in, down to processed analog AF-out, is performed on a single chip. Signal conforming to the standard by the Broadcast Television Systems Committee (BTSC).

The DBX noise reduction, or alternatively, MICRONAS Noise Reduction (MNR) is performed alignment free. Other processed standards are the Japanese FM-FM multiplex standard (EIA-J) and the FM Stereo Radio standard.

6.SOUND OUTPUT STAGE WITH TDA7480L

The TDA7480L is an audio class-D amplifier assembled in Power DIP package specially designed for high efficiency applications mainly for TV and Home Stereo sets.

Mute stand-by function of the audio amplifier can be described as the following; the pin 12 (MUTE/STAND-BY) controls the amplifier status by two different thresholds, referred to ground. When Vpin 12 voltage is lower than 0.7V the amplifier is in Stand-by mode and the final stage generators are off. When Vpin 12 is higher than 4V, the amplifier is in play mode.

The TDA7480L is a 10W+10W stereo sound amplifier with mute/stand-by facility. MUTE control signal coming from microcontroller (when it is at high level) activates the mute function. IC is muted when mute pin is at low level (pin12). MUTE pin can also be activated via an external pop-noise circuitry in order to eliminate pop noise when TV is turned off. Just after the TV is turned off, this circuit switches the IC to stand-by mode by pulling the mute pin voltage to ground.

7.VERTICAL OUTPUT STAGE WITH TDA8177F

The IC TDA8177F is the vertical deflection booster circuit. Two supply voltages, +12V and -12V are needed to scan the inputs VERT+ and VERT-, respectively. And a third supply voltage, +60V for the flyback limiting are needed. The vertical deflection coil is connected in series between the output and feedback to the input.

8.VIDEO OUTPUT AMPLIFIER TDA6109

The TDA6109 includes three video output amplifiers in order to drive the three cathodes of a colour picture tube directly. To obtain maximum performance, the amplifier is used with black-current control.

9.POWER SUPPLY (SMPS)

The DC voltages required at various parts of the chassis are provided by an SMPS transformer controlled by the IC MC44608, which is designed for driving, controlling and protecting switching transistor of SMPS. The transformer generates 135V for FBT input, +/-14V for audio amplifier, 8V stand by voltage and 8V, 12V and 5V supplies for other different parts of the chassis.

An optocoupler is used to control the regulation of line voltage and stand-by power consumption. There is a regulation circuit in secondary side. This circuit produces a control voltage according to the changes in 135V DC voltage, via an optocoupler (TCET 1102G) to pin3 of the IC.

During the switch on period of the transistor, energy is stored in the transformer. During the switch off period energy is fed to the load via secondary winding. By varying switch-on time of the power transistor, it controls each portion of energy transferred to the second side such that the output voltage remains nearly independent of load variations.

10.MICROCONTROLLER SDA5550

10.1.General Features

• Feature selection via special function register
• Simultaneous reception of TTX, VPS, PDC, and WSS (line 23)
• Supply Voltage 2.5 and 3.3 V
• ROM version is used.

10.2.External Crystal and Programmable Clock Speed

• Single external 6MHz crystal, all necessary clocks are generated internally
• CPU clock speed selectable via special function registers.
• Normal Mode 33.33 MHz CPU clock, Power Save mode 8.33 MHz

10.3.Microcontroller Features

• 8bit 8051 instruction set compatible CPU.
• 33.33-MHz internal clock (max.)
• 0.360 ms (min.) instruction cycle
• Two 16-bit timers
• Watchdog timer
• Capture compare timer for infrared remote control decoding
• Pulse width modulation unit (2 channels 14 bit, 6 channels 8 bit)
• ADC (4 channels, 8 bit)
• UART (rxd, txd)

10.4.Memory

• Up to 128 Kilobyte on Chip Program ROM
• Eight 16-bit data pointer registers (DPTR)
• 256-bytes on-chip Processor Internal RAM (IRAM)
• 128bytes extended stack memory.
• Display RAM and TXT/VPS/PDC/WSS-Acquisition-Buffer directly accessible via MOVX
• UP to 16KByte on Chip Extended RAM (XRAM) consisting of;
- 1 Kilobyte on-chip ACQ-buffer-RAM (access via MOVX)
- 1 Kilobyte on-chip extended-RAM (XRAM, access via MOVX) for user software
- 3 Kilobyte Display Memory

10.5.Display Features

• ROM Character set supports all East and West European Languages in single device
• Mosaic Graphic Character Set
• Parallel Display Attributes
• Single/Double Width/Height of Characters
• Variable Flash Rate
• Programmable Screen Size (25 Rows x 33...64 Columns)
• Flexible Character Matrixes (HxV) 12 x 9...16
• Up to 256 Dynamical Redefinable Characters in standard mode; 1024 Dynamical Redefinable Characters in Enhanced Mode
• CLUT with up to 4096 colour combinations
• Up to 16 Colours per DRCS Character
• One out of 8 Colours for Foreground and Background Colours for 1-bit DRCS and ROM Characters

10.6.ROM Characters
• Shadowing
• Contrast Reduction
• Pixel by Pixel Shiftable Cursor With up to 4 Different Colours
• Support of Progressive Scan and 100 Hz.
• 3 X 4Bits RGB-DACs On-Chip
• Free Programmable Pixel Clock from 10 MHz to 32MHz
• Pixel Clock Independent from CPU Clock
• Multinorm H/V-Display Synchronization in Master or Slave Mode

10.7.Acquisition Features
• Multi-standard Digital Data Slicer
• Parallel Multi-norm Slicing (TTX, VPS, WSS, CC, G+)
• Four Different Framing Codes Available
• Data Caption only limited by available Memory
• Programmable VBI-buffer
• Full Channel Data Slicing Supported
• Fully Digital Signal Processing
• Noise Measurement and Controlled Noise Compensation
• Attenuation Measurement and Compensation
• Group Delay Measurement and Compensation
• Exact Decoding of Echo Disturbed Signals

10.8.Ports
• One 8-bit I/O-port with open drain output and optional I^2C Bus emulation support (Port0)
• Two 8-bit multifunction I/O-ports (Port1, Port3)
• One 4-bit port working as digital or analogue inputs for the ADC (Port2)
• One 2-bit I/O port with secondary function (P4.2, 4.3, 4.7)
• One 4-bit I/O-port with secondary function (P4.0, 4.1, 4.4) (Not available in P-SDIP 52)

11.SERIAL ACCESS 32K EEPROM

24LC32 is the 32Kbit electrically erasable programmable memory. The memory is compatible with the I^2C standard, two wire serial interface, which uses a bi-directional data bus and serial clock.

12.CLASS AB STEREO HEADPHONE DRIVER TDA1308

The TDA1308 is an integrated class AB stereo headphone driver contained in a DIP8 plastic package. The device is fabricated in a 1 mm CMOS process and has been primarily developed for portable digital audio applications.

13.SAW FILTERS

K3953M:
Standard
B/G, D/K, I, L/L'
Features
TV IF video filter with Nyquist slopes at 33,90 MHz and 38,90 MHz
Constant group delay
Suitable for CENELEC EN 55020
Terminals
Tinned CuFe alloy
Pin configuration
1 Input
2 Input - ground
3 Chip carrier - ground
4 Output
5 Output

K3958M:
Standard
B/G, D/K, I, L/L'
Features
TV IF video filter with Nyquist slopes at 33.90 MHz and 38.90 MHz
Constant group delay
Terminal and Pin configuration are the same with K3953M

K9356M:
Standard
B/G, D/K, I, L
Features
TV IF audio filter with pass band for sound carriers at 32,40 MHz (D/K, L), 32,90 MHz (I) and 33,40 MHz (B/G)
Terminal and Pin configuration are the same with K3953M

K9656M:
Standard
B/G, D/K, I, L/L'
Features
TV IF audio filter with two channels
Channel 1 (L') with one pass band for sound carriers at 40,40 MHz (L') and 39,75 MHz (L'- NICAM)
Channel 2 (B/G, D/K, L, I) with one pass band for sound carriers between 32,35 MHz and 33,40 MHz
Terminal and Pin configuration are the same with K3953M

14.IC DESCRIPTIONS

TDA6109	27W401
24LC32	SDA5275
DRAM 4MX4	SDA9400
LM317T	DDP3310
SDA5550	TEA6415
VPC3230D	TDA1308T
MSP3411G	TL431
TDA9885/86	LM7808
TDA8177F	LM1086
MC44608	TCET1102G
TDA7480L	SAA3010T

14.1.TDA6109

14.1.1.General Description

The TDA6109JF includes three video output amplifiers in one plastic DIL-bent-SIL 9-pin medium power (DBS9MPF) package (SOT111-1), using high-voltage DMOS technology, and is intended to drive the three cathodes of a colour CRT directly. To obtain maximum performance, the amplifier should be used with black-current control.

14.1.2.Features

· Typical bandwidth of 9.0 MHz for an output signal of 60 V (p-p)
· High slew rate of 1850 V/ms
· No external components required
· Very simple application
· Single supply voltage of 200 V
· Internal reference voltage of 2.5 V
· Fixed gain of 51
· Black-Current Stabilization (BCS) circuit
· Thermal protection

14.1.3.Pinning

SYMBOL	PIN	DESCRIPTION
$V_{i(1)}$	1	inverting input 1
$V_{i(2)}$	2	inverting input 2
$V_{i(3)}$	3	inverting input 3
GND	4	ground (fin)
I_{om}	5	black current measurement output
V_{DD}	6	supply voltage
$V_{oc(3)}$	7	cathode output 3
$V_{oc(2)}$	8	cathode output 2
$V_{oc(1)}$	9	cathode output 1

14.2.27W401

14.2.1.Description

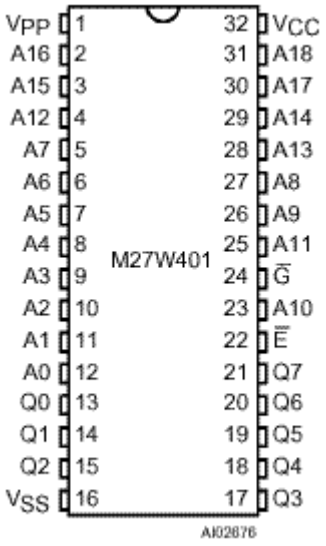
The M27W401 is a low voltage 4 Mbit EPROM offered in the two ranges UV (ultra violet erase) and OTP (one time programmable). It is ideally suited for microprocessor systems requiring large data or program storage and is organized as 524,288 by 8 bits. The M27W401 operates in the read mode with a supply voltage as low as 2.7V at –40 to 8??C temperature range. The decrease in operating power allows either a reduction of the size of the battery or an increase in the time between battery re-charges.

The FDIP32W (window ceramic frit-seal package) has a transparent lid, which allows the user to ex-pose the chip to ultraviolet light to erase the bit pat-tern. A new pattern can then be written to the device by following the programming procedure. For application where the content is programmed only one time and erasure is not required, the M27W401 is offered in PDIP32, PLCC32 and TSOP32 (8x20 mm) packages.

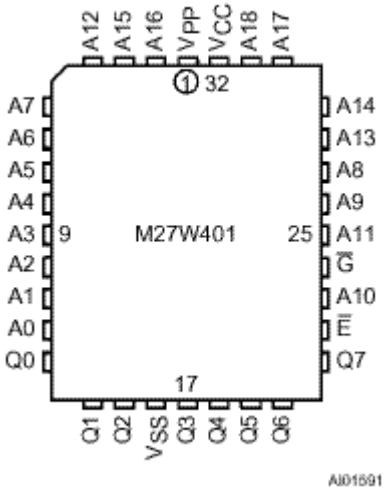
14.2.2.Features

2.7V to 3.6v Low voltage in Read Operation
Access time:
–70ns at V_{CC} = 3.0V to 3.6V
–80ns at V_{CC} = 2.7V to 3.6V
Pin Compatible with M27C4001
Low Power Consumption:
–1?mA max Standby Current
– 15mA max Active Current at 5MHz
Programming Time 10?ns/byte
High Reliability CMOS Technology
– 2,000V ESD Protection
– 200mA Latchup Protection Immunity
Electronic Signature
– Manufacturer Code: 20h
– Device Code: 41h

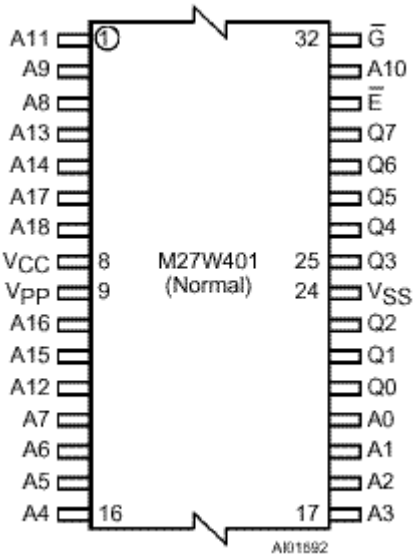
14.2.3.Connections



DIP connections



LCC Connections



TSOP Connections

Signal Names

A0-A18	Address Inputs
Q0-Q7	Data Outputs
E	Chip Enable
G	Output Enable
V_{pp}	Program Supply
V_{cc}	Supply Voltage
V_{ss}	Ground

14.3.24LC32A

14.3.1.Description

The Microchip Technology Inc. 24LC32A is a 4K x 8 (32K bit) Serial Electrically Erasable PROM capable of operation across a broad voltage range (2.5V to 6.0V). It has been developed for advanced, low power applications such as personal communications or data acquisition. The 24LC32A also has a page-write capability of up to 32 bytes of data. The 24LC32A is capable of both random and sequential reads up to the 32K boundary. Functional address lines allow up to eight 24LC32A devices on the same bus, for up to 256K bits address space. Advanced CMOS technology and broad voltage range make this device ideal for low-power/ low-voltage, nonvolatile code and data applications. The 24LC32A is available in the standard 8-pin plastic DIP and both 150 mil and 200 mil SOIC packaging.

14.3.2.Features

• Single supply with operation down to 2.5V
• Maximum write current 3 mA at 6.0V
• Standby current 1 mA max at 2.5V
• 2-wire serial interface bus, I 2 CÔ compatible
• 100 kHz (2.5V) and 400 kHz (5V) compatibility
• Self-timed ERASE and WRITE cycles
• Power on/off data protection circuitry
• Hardware write protect
• 1,000,000 Erase/Write cycles guaranteed
• 32 byte page or byte write modes available
• Schmitt trigger filtered inputs for noise suppression
• Output slope control to eliminate ground bounce
• 2 ms typical write cycle time, byte or page
• Up to eight devices may be connected to the same bus for up to 256K bits total memory
• Electrostatic discharge protection > 4000V
• Data retention > 200 years
• 8-pin PDIP and SOIC packages
• Temperature ranges
• Commercial (C): 0°C to +75°C
• Industrial (I): -40°C to +85°C

14.3.3.Pin Descriptions

A0, A1, A2 Chip Address Inputs

The A0..A2 inputs are used by the 24LC32A for multiple device operation and conform to the 2-wire bus standard. The levels applied to these pins define the address block occupied by the device in the address map. A particular device is selected by transmitting the corresponding bits (A2, A1, A0) in the control byte.

SDA Serial Address/Data Input/Output

This is a Bi-directional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pull up resistor to VCC (typical 10 kO for 100 kHz, 2 kO for 400 kHz) For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL HIGH are reserved for indicating the START and STOP conditions.

SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

WP
This pin must be connected to either VSS or VCC. If tied to VSS, normal memory operation is enabled (read/write the entire memory 000-FFF). If tied to VCC, WRITE operations are inhibited. The entire memory will be write-protected. Read operations are not affected.
WCC
+2.5V to 6V Power Supply
WSS
Ground

14.4.SDA5275

14.4.1.Features

• Single chip teletext IC
• Analog CVBS-input with onchip clamping circuitry
• Slicer
• Supports level 1, 2.5 and 3.5 ETSI teletext standard
• Stores up to 14 teletext pages on chip
• Stores up to 2048 teletext pages with external 16 M memory
• SDA 5275: full level 2.5 processing
• Analog RGB-output
• 41 Latin script languages
• 12 ´ 10 character size
• Parallel display attributes
• 64 from 4096 colors selectable
• Enhanced flash modes
• Dynamically redefinable character set (DRCS, PCS)
• Pixel graphics
• Full screen display (64 ´ 32 or 80 ´ 24 character positions)
• Horizontal and vertical scrolling
• Graphic cursors
• 4:3 and 16:9 display
• Multinorm display (50/60/100/120 Hz)
• RISC-processor
• Firmware downloadable
• I^2C / 3 wire UART-interface (1 Mbit/s)
• Independent clocks for acquisition and display
• Tools for greatly simplified software development
• 24-Kbyte on-chip reconfigurable DRAM
• 44160-bit character ROM
• One external crystal for all standards

14.4.2.Pin Definition and functions

Pin No. P-LCC-68-1	Symbol	Function
1	INTQ	Interrupt request output to ext. controller
2	CLK-IO	System clock input/output
3	TCSQ/FLD	Composite sync output/ field output
4	VS/VCS	Vertical sync input/output
5	HS	Horizontal sync input/output
6	XOUT	20.5-MHz crystal oscillator output
7	XIN	20.5-MHz crystal oscillator input
8	GPO	General purpose output
9	TM	Test pin, leave open or connect VSS
10	CVBS	CVBS-video signal input
11	VDD1	+ 5 V digital supply
12	VDDA	+ 5 V analog supply
13	VSSA1	Analog ground
14	N.C.	Not connected
15	N.C.	Not connected
16	VDD2	+ 5 V digital supply
17	RES	Chip reset
18	N.C.	Not connected

19	N.C.	Not connected
20	N.C.	Not connected
21	VDD3	+ 5 V digital supply
22	N.C.	Not connected
23	VREF	+ 3 V reference voltage input
24	N.C.	Not connected
25	VDD4	+ 5 V digital supply
26	A8	External DRAM-address
27	A7	External DRAM-address
28	A6	External DRAM-address
29	A5	External DRAM-address
30	A4	External DRAM-address
31	A3	External DRAM-address
32	A2	External DRAM-address
33	A1	External DRAM-address
34	A0	External DRAM-address
35	A9	External DRAM-address
36	A10	External DRAM-address
37	A11	External DRAM-address
38	RASQ	Row address strobe (DRAM)
39	WEQ	Write enable (DRAM)
40	D1	External DRAM-data
41	D0	External DRAM-data
42	D2	External DRAM-data
43	D3	External DRAM-data
44	VSS4	0 V digital supply
45	CASQ	Column address strobe
46	N.C.	Not connected
47	N.C.	Not connected
48	N.C.	Not connected
49	VSS3	0 V digital supply
50	N.C.	Not connected
51	N.C.	Not connected
52	N.C.	Not connected
53	N.C.	Not connected
54	N.C.	Not connected
55	VSS2	0 V digital supply
56	VBB	Substrate bias voltage N.C.* (depends on version)
57	N.C.	Not connected
58	VSSA2	Analog ground
59	RGB-GND	RGB-ground
60	VSS1	0 V digital supply
61	R	Analog red display output
62	G	Analog green display output
63	B	Analog blue display output
64	BLAN	Blanking signal open drain output
65	CORQ	Contrast reduction open drain output
66	SCL	Bi-directional I^2C Bus clock port
67	SDA	Bi-directional I^2C Bus data port
68	I^2CEN	I^2C Bus enable

14.5.DRAM 4MX4

14.5.1.General Description

The 4 Meg x 4 DRAM is a randomly accessed, solid-state memory containing 16,777,216 bits organized in a x4 con-figuration. RAS# is used to latch the row address (first 11 bits for 2K and first 12 bits for 4K). Once the page has been opened by RAS#, CAS# is used to latch the column address (the latter 11 bits for 2K and the latter 10 bits for 4K, address pins A10 and A11 are “don’t care”). READ and WRITE cycles are selected with the WE# input. A logic HIGH on WE# dictates READ mode, while a logic LOW on WE# dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE# or CAS#, whichever occurs last. An EARLY WRITE occurs when WE# is taken LOW prior to CAS# falling. A LATE WRITE or READ-MODIFY-WRITE occurs when WE# falls after CAS# is taken LOW. During EARLY WRITE cycles, the data outputs (Q) will remain High-Z regardless of the state of OE#. During LATE WRITE or READ-MODIFY-WRITE cycles, OE# must be taken HIGH to disable the

data outputs prior to applying input data. If a LATE WRITE or READ-MODIFY-WRITE is attempted while keeping OE# LOW, no write will occur, and the data outputs will drive read data from the accessed location. The four data inputs and the four data outputs are routed through four pins using common I/O, and pin direction is controlled by WE# and OE#.

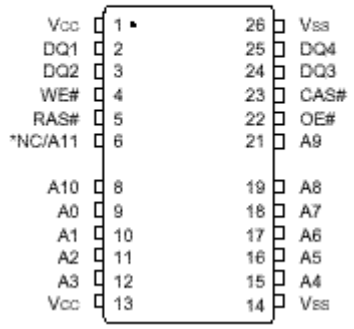
14.5.2.Features

- Industry-standard x4 pin out, timing, functions and packages
- State-of-the-art, high-performance, low-power CMOS silicon-gate process
- Single power supply (+3.3V ±0.3V or +5V ±10%)
- All inputs, outputs and clocks are TTL-compatible
- Refresh modes: RAS#-ONLY, HIDDEN and CAS#-BEFORE- RAS# (CBR)
- Optional Self Refresh (S) for low-power data retention
- 11 row, 11 column addresses (2K refresh) or 12 row, 10 column addresses (4K refresh)
- Extended Data-Out (EDO) PAGE MODE access cycle
- 5V-tolerant inputs and I/Os on 3.3V devices

14.5.3.Pin Assignment

Top View

24/26-Pin SOJ
(DA-2)



*NC on 2K refresh and A11 on 4K refresh options. **Note:** The “#” symbol indicates signal is active LOW.

14.6.SDA9400

14.6.1.General Description

The SDA9400 is a new component of the Micronas MEGAVISION ® IC set in a 0.35µm embedded DRAM technology (frame memory embedded). The SDA9400 is pin compatible to the SDA9401 (field memory embedded). The SDA9400 comprises all main functionalities of a digital feature box in one monolithic IC. The scan rate conversion to 100/120 Hz interlaced (50/60 Hz progressive) is based on a motion adaptive algorithm. The scan rate converted picture can be vertically expanded. The SDA9400 has a free running mode, therefore features like scan rate conversion to e.g. 70, 75 Hz with joint lines or multiple picture display (e.g. tuner scan) are possible. Due to the frame based signal processing, the noise reduction has been greatly improved. Furthermore separate motion detectors for luminance and chrominance have been implemented. For automatic controlling of the noise reduction parameters a noise measurement algorithm is included, which measures the noise level in the picture or in the blanking period. In addition a spatial noise reduction is implemented, which reduces the noise even in the case of motion. The input signal can be compressed horizontally and vertically with a certain number of factors. Therefore split screen is supported. Beside these additional functions like coloured background, windowing and flashing are implemented.

14.6.2.Features

- **Two input data formats**

- 4:2:2 luminance and chrominance parallel (2 x 8 wires)
- ITU-R 656 data format (8 wires)

• Two different representations of input chrominance data
- 2‘s complement code
- Positive dual code
• Flexible input sync controller
• Flexible compression of the input signal
- Digital vertical compression of the input signal (1.0, 1.25, 1.5, 1.75, 2.0, 3.0, 4.0)
- Digital horizontal compression of the input signal (1.0, 2.0, 4.0)
• Noise reduction
- Motion adaptive spatial and temporal noise reduction (3D-NR)
- Temporal noise reduction for luminance frame based or field based
- Temporal noise reduction for chrominance field based
- Separate motion detectors for luminance and chrominance
- Flexible programming of the temporal noise reduction parameters
- Automatic measurement of the noise level (5-bit value, readable by I²C bus)
• 3-D motion detection
- High performance motion detector for scan rate conversion
- Global motion detection flag (readable by I²C bus)
- Movie mode and phase detector (readable by I²C bus)
• TV mode detection by counting line numbers (PAL, NTSC, readable by I²C bus)
• Embedded memory
- 5 Mbit embedded DRAM core for field memories
- 192 kbit embedded DRAM core for line memories
• Flexible clock and synchronization concept
- Decoupling of the input and output clock system possible
• Scan rate conversion
- Motion adaptive 100/120 Hz interlaced scan conversion
- Motion adaptive 50/60 Hz progressive scan conversion
- Simple static interlaced and progressive conversion modes for 100/120 Hz interlaced or 50/60 Hz progressive scan conversion: e.g. ABAB, AABB, AA*B*B, AAAA, BBBB, AB, AA*
- Simple progressive scan conversion with joint lines:
50 Hz -> 60, 70, 75 Hz progressive
60 Hz -> 70, 75 Hz progressive
- Large area and line flicker reduction
• Flexible digital vertical expansion of the output signal (1.0, ... [1/32] ..., 2.0)
• Flexible output sync controller
- Flexible positioning of the output signal
- Flexible programming of the output sync raster
- External synchronization by backend IC possible
(e.g. split screen for one TV channel with joint lines and one PC VGA channel)
• Signal manipulations
- Insertion of coloured background
- Vertical and/or horizontal windowing with four different speed factors
- Flash generation (for supervising applications, motion flag readable by I²C bus)
- Still frame or field
- Support of split screen applications
- Multiple picture display - Tuner scan (4 and 16 times for 4:3, 12 times for 16:9 tubes)
- Support of multi picture display with PIP or front-end processor with integrated scaler
(e.g. 9 times display of PIP pictures, picture tracking, random pictures, still-in-moving picture, moving-in-still picture)
• I²C-bus control (400 kHz)
• P-MQFP-64 package
• 3.3 V ± 5% supply voltage

14.6.3.Pin Definition

Pin No.	Name	Type	Description
2,8,24,42,55	VSS1	S	Supply voltage (V_{SS} = 0 V)
9,25,41,56	VDD1	S	Supply voltage (V_{DD} = 3.3 V)
36,52,58	VSS2	S	Supply voltage (V_{SS} = 0 V)
35,51,53,57,59	VDD2	S	Supply voltage (V_{DD} = 3.3 V)
43,..,50	YIN0...7	I/TTL	Data input Y (see input data format)
31,..,34;37,...,40	UVIN0...7	I/TTL	Data input UV (for 4:2:2 parallel, see input data format)

		PD	(for CCIR 656, see input data format)
30	RESET	I/TTL	System reset. The RESET input is low active. In order to ensure correct operation a "Power On Reset" must be performed. The RESET pulse must have a minimum duration of two clock periods of the system clock CLK1.
23	HIN	I/TTL PD	H-Sync input (only for full CCIR 656)
22	VIN	I/TTL PD	V-Sync input (only for full CCIR 656)
29	SYNCEN	I/TTL	Synchronization enable input
21	SDA	I/O	I^2C-Bus data line (5V ability)
20	SCL I	I	I^2C-Bus clock line (5V ability)
54	CLK1	I/TTL	System clock 1
17,..,10	UVOUT0...7	O/TTL	Data output UV (see output data format)
7,..,3;1;64;63	YOUT0...7	O/TTL	Data output Y (see output data format)
62	HREF	O/TTL	Horizontal active video output
61	VOUT/ VEXT	I/O/ TTL	EXSYN=0 (I^2C-bus parameter): V-Sync output EXSYN=1: External V-Sync input for output part
60	HOUT/ HEXT	I/O/ TTL	EXSYN=0 (I^2C-bus parameter): H-Sync output EXSYN=1: External H-Sync input for output part
18	INTERLACED	O/TTL	Interlace signal for AC coupled vertical deflection
28	X1 / CLK2	I/TTL	Crystal connection / System clock 2
27	X2	O/AN	Crystal connection
26	CLKOUT	O/TTL	Clock output (depends on I^2C parameters CLK11EN, CLK21EN, FREQR)
19	TEST	I/TTL	Test input, connect to *V* SS for normal operation

14.7.LM317T

14.7.1.Description

The LM317T is an adjustable 3 terminal positive voltage regulator capable of supplying in excess of 1.5 amps over an output range of 1.25 to 37 volts. This voltage regulator is exceptionally easy to use and requires only two external resistors to set the output voltage. Further, it employs internal current limiting, thermal shutdown and safe area compensation, making it essentially blow–out proof. The LM317 serves a wide variety of applications including local, on card regulation. This device can also be used to make a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM317 can be used as a precision current regulator.

14.7.2.Features

- Output Current in Excess of 1.5 A
- Output Adjustable between 1.2 V and 37 V
- Internal Thermal Overload Protection
- Internal Short Circuit Current Limiting Constant with Temperature
- Output Transistor Safe–Area Compensation
- Floating Operation for High Voltage Applications
- Available in Surface Mount D^2PAK, and Standard 3–Lead Transistor Package
- Eliminates Stocking many Fixed Voltages

14.8.DDP3310

14.8.1.Description

The DDP 3310B is a single-chip digital Display and Deflection Processor designed for high-quality back-end applications in 100/120-Hz TV sets with 4:3 or 16:9 picture tubes. The IC can be combined with members of the DIGIT 3000 IC family (VPC 32xx, TPU 3040), or it can be used with third-party products. The IC contains the entire digital video component and deflection processing and all analog interface components.

14.8.2.Features

Video processing

– linear horizontal scaling (0.25 … 4)
– non-linear horizontal scaling “panorama-vision”
– dynamic peaking

– soft limiter (gamma correction)
– color transient improvement
– programmable RGB matrix
– picture frame generator
– two analog RGB/Fast-Blank inputs. The DDP 3310B is a single-chip digital Display and Deflection Processor designed for high-quality back-

Deflection processing
– scan velocity modulation output
– high-performance H/V deflection
– EHT compensation for vertical / East/West
– soft start/stop of H-Drive
– vertical angle and bow
– differential vertical output
– vertical zoom via deflection
– horizontal and vertical protection circuit
– adjustable horizontal frequency for VGA/SVGA display

Miscellaneous
– selectable 4:1:1/ 4:2:2 YC $_r$ C $_b$ input
– selectable 27/ 32-MHz line-locked clock input
– crystal oscillator for horizontal protection
– automatic picture tube adjustment (cutoff, white-drive)
– single 5-V power supply
– hardware for simple 50/60-Hz to 100/ 120-Hz conversion (display frequency doubling)
– two I^2C-controlled PWM outputs
– beam current limiter

14.8.3.Pin connection and short descriptions

NC = not connected
X = obligatory; connect as described in circuit diagram
OUT = Output
LV = if not used, leave vacant
IN = Input
SUPPLY = Supply Pin

Pin no PLCCK 68 pin	Pin name	Type	Connection (if not used)	Short description
1	VSUPP	SUPPLY	X	Supply voltage, Output pin driver
2	GNDP	SUPPLY	X	Ground, Output pin driver
3	VS2	IN	GNDD	Additional VSYNC input
4	FIFORRD	OUT	LV	FIFO Read counter reset
5	FIFORD	OUT	LV	FIFO Read Enable
6	FIFOWR	OUT	LV	FIFO Write Enable
7	FIFORWR	OUT	LV	FIFO Write counter reset
8	HOUT	OUT	X	Horizontal Drive Output
9	HFLB	IN	Hout	Horizontal Flyback Input
10	SAFETY	IN	GNDO	Safety Input
11	VPROT	IN	GNDO	Vertical protection Input
12	FREQSEL	IN	X	Selection of H-Drive Frequency Range
13	CM1	IN	X	Clock select 40.5 or 27/32 MHz
14	CMO	IN	X	Clock select 27/32 MHz
15	RSW2	OUT	LV	Range Switch2, Measurement ADC
16	RSW1	IN/OUT	LV	Range Switch1, Measurement ADC
17	SENSE	IN	GNDO	Sense ADC Input
18	GNDM	SUPPLY	X	Ground, MADC Input
19	VERT+	OUT	GNDO	Differantial Vertical Sawtooth Output
20	VERT-	OUT	GNDO	Differantial Vertical Sawtooth Output
21	EW	OUT	GNDO	Vertical Parabola Output
22	XREF	IN	X	Reference Input for RGB DACs
23	SVM	OUT	VSUPO	Scan Velocity Modulation
24	ROUT	OUT	VSUPO	Analog Output Red
25	GOUT	OUT	VSUPO	Analog Output Green
26	BOUT	OUT	VSUPO	Analog Output Blue
27	GNDO	SUPPLY	X	Ground, Analog Back-end
28	VSUPO	SUPPLY	X	Supply Voltage, Analog Back-end

29	VRD/BCS	IN	X	DAC Reference, Beam Current Safety
30	FBLIN1	IN	GNDO	Fast-Blank1 Input
31	RIN1	IN	GNDO	Analog Red1 Input
32	GIN1	IN	GNDO	Analog Green1 Input
33	BIN1	IN	GNDO	Analog Blue1 Input
34	FBLIN2	IN	GNDO	Fast-Blank2 Input
35	RIN2	IN	GNDO	Analog Red2 Input
36	GIN2	IN	GNDO	Analog Green2 Input
37	BIN2	IN	GNDO	Analog Blue2 Input
38	TEST	IN	GNDD	Test Pin
39	RESQ	IN	X	Reset Input, active low
40	PWM1	OUT	LV	I^2C-controlled DAC
41	PWM2	OUT	LV	I^2C-controlled DAC
42	HCS	IN	GNDD	Half-contrast
43	C0	IN	GNDD	Picture Bas Chroma (LSB)
44	C1	IN	GNDD	Picture Bas Chroma
45	C2	IN	GNDD	Picture Bas Chroma
46	C3	IN	GNDD	Picture Bas Chroma
47	C4	IN	GNDD	Picture Bas Chroma
48	C5	IN	GNDD	Picture Bas Chroma
49	C6	IN	GNDD	Picture Bas Chroma
50	C7	IN	GNDD	Picture Bas Chroma (MSB)
51	VSUPD	SUPPLY	X	Supply Voltage, Digital Circuitry
52	GNDD	SUPPLY	X	Ground, Digital Circuitry
53	LLC2	IN	X	System Clock Input (27/32/40.5 MHz)
54	Y0	IN	GNDD	Picture Bas Luma (LSB)
55	Y1	IN	GNDD	Picture Bas Luma
56	Y2	IN	GNDD	Picture Bas Luma
57	Y3	IN	GNDD	Picture Bas Luma
58	Y4	IN	GNDD	Picture Bas Luma
59	Y5	IN	GNDD	Picture Bas Luma
60	Y6	IN	GNDD	Picture Bas Luma
61	Y7	IN	GNDD	Picture Bas Luma (MSB)
62	LLC1	IN	VSUPD	Single Line-Locked Clock Input (13.5/16 MHz)
63	HS	IN	X	Horizontal Sync Input
64	VS	IN	GNDD	Vertical Sync Input
65	XTALK2	OUT	X	Analog Crystal Output (5-MHz Security Clock)
66	XTALK1	IN	X	Analog Crystal Input (5-MHz Security Clock)
67	SDA	IN/OUT	X	I^2C-Bus Data
68	SCL	IN/OUT	X	I^2C-Bus Clock

14.9.SDA5550

14.9.1.General definition

The SDA5550M is a single chip teletext decoder for decoding World System Teletext data as well as Video Programming System (VPS), Program Delivery Control (PDC), and Wide Screen Signalling (WSS) data used for PAL plus transmissions (Line 23). The device provides an integrated general-purpose, fully 8051-compatible Microcontroller with television specific hardware features. Microcontroller has been enhanced to provide powerful features such as memory banking, data pointers, and additional interrupts etc. The on-chip display unit for displaying Level 1.5 teletext data can also be used for customer defined on screen displays. Internal XRAM consists of up to 17 Kbytes. This device can support external memory up to 1Mbyte ROM and RAM.TVTEXT Controller contains a data slicer for VPS, WSS, PDC and TXT, an acceleration acquisition hardware module, a display generator for Level 1.5 TXT and powerful On screen Display capabilities based on parallel attributes, and pixel oriented characters (DRCS). The 8 bit Microcontroller operates at 360nsec cycle time (min). Controller with dedicated hardware does most of the internal TXT acquisition processing, transfer data to/from external memory interface and receives/transmits data via I^2C-firmware user interface. SDA5550M is realized in 0.25 micron technology with 2.5V supply voltage and 3.3V I/O compatible. The IC produces the following input or output control signals; AGC_CON, MODE_SW, L / L', PIP_MODS, PIP_SEL, ON/OFF (stand-by), SC1..3_IN_AV (pin 8 information from 3 SCARTs), AFC, MUTE (to mute audio output IC), I^2CEN.

14.9.2.Features

General

• Feature selection via special function register
• Simultaneous reception of TTX, VPS, PDC, and WSS (line 23)
• Supply Voltage 2.5 and 3.3 V

External Crystal and Programmable clock speed

Single external 6MHz crystal, all necessary clocks are generated internally
CPU clock speed selectable via special function registers.
Normal Mode 33.33 MHz CPU clock, Power Save mode 8.33 MHz

Microcontroller Features

• 8bit 8051 instruction set compatible CPU.
• 33.33-MHz internal clock (max.)
• 0.360ms (min.) instruction cycle
• Two 16-bit timers
• Watchdog timer
• Capture compare timer for infrared remote control decoding
• Pulse width modulation unit (2 channels 14 bit, 6 channels 8 bit)
• ADC (4 channels, 8 bit)
• UART

Memory

• Non-multiplexed 8-bit data and 16 … 20-bit address bus (ROMless Version)
• Memory banking up to 1Mbyte (Romless version)
• Up to 128 Kilobyte on Chip Program ROM
• Eight 16-bit data pointer registers (DPTR)
• 256-bytes on-chip Processor Internal RAM (IRAM)
• 128bytes extended stack memory.
• Display RAM and TXT/VPS/PDC/WSS-Acquisition-Buffer directly accessible via MOVX
• UP to 16KByte on Chip Extended RAM (XRAM) consisting of;
- 1 Kilobyte on-chip ACQ-buffer-RAM (access via MOVX)
- 1 Kilobyte on-chip extended-RAM (XRAM, access via MOVX) for user software
- 3 Kilobyte Display Memory

Display Features

• ROM Character Set Supports all East and West European Languages in single device
• Mosaic Graphic Character Set
• Parallel Display Attributes
• Single/Double Width/Height of Characters
• Variable Flash Rate
• Programmable Screen Size (25 Rows x 33...64 Columns)
• Flexible Character Matrixes (HxV) 12 x 9...16
• Up to 256 Dynamical Redefinable Characters in standard mode; 1024 Dynamical Redefinable Characters in Enhanced Mode
• CLUT with up to 4096 color combinations
• Up to 16 Colors per DRCS Character
• One out of Eight Colors for Foreground and Background Colors for 1-bit DRCS and ROM Characters
• Shadowing
• Contrast Reduction
• Pixel by Pixel Shiftable Cursor With up to 4 Different Colors
• Support of Progressive Scan and 100 Hz.
• 3 X 4Bits RGB-DACs On-Chip
• Free Programmable Pixel Clock from 10 MHz to 32MHz
• Pixel Clock Independent from CPU Clock
• Multinorm H/V-Display Synchronization in Master or Slave Mode

Acquisition Features

- Multistandard Digital Data Slicer
- Parallel Multi-norm Slicing (TTX, VPS, WSS, CC, G+)
- Four Different Framing Codes Available
- Data Caption only Limited by available Memory
- Programmable VBI-buffer
- Full Channel Data Slicing Supported
- Fully Digital Signal Processing
- Noise Measurement and Controlled Noise Compensation
- Attenuation Measurement and Compensation
- Group Delay Measurement and Compensation
- Exact Decoding of Echo Disturbed Signals

Ports

- One 8-bit I/O-port with open drain output and optional I^2C Bus emulation support (Port 0)
- Two 8-bit multifunction I/O-ports (Port 1, Port 3)
- One 4-bit port working as digital or analog inputs for the ADC (Port 2)
- One 2-bit I/O port with secondary functions (P4.2, 4.3, 4.7)
- One 4-bit I/O-port with secondary function (P4.0, 4.1, 4.4) (Not available in P-SDIP 52)

14.10.TEA6415C

14.10.1.General Description

The main function of the IC is to switch 8 video input sources on 6 outputs. Each output can be switched on only one of each input. On each input an alignment of the lowest level of the signal is made (bottom of synch. top for CVBS or black level for RGB signals). Each nominal gain between any input and output is 6.5dB. For D2MAC or Chroma signal the alignment is switched off by forcing, with an external resistor bridge, 5 V_{DC} on the input. Each input can be used as a normal input or as a MAC or Chroma input (with external resistor bridge). All the switching possibilities are changed through the BUS. Driving 75? load needs an external transistor. It is possible to have the same input connected to several outputs. The starting configuration upon power on (power supply: 0 to 10V) is undetermined. In this case, 6 words of 16 bits are necessary to determine one configuration. In other case, 1 word of 16 bits is necessary to determine one configuration.

14.10.2.Features

- 20MHz Bandwidth
- Cascadable with another TEA6415C (Internal address can be changed by pin 7 voltage)
- 8 Inputs (CVBS, RGB, MAC, CHROMA,...)
- 6 Outputs
- Possibility of MAC or chroma signal for each input by switching-off the clamp with an external resistor bridge
- Bus controlled
- 6.5dB gain between any input and output
- 55dB crosstalk at 5mHz
- Fully ESD protected

14.10.3.Pinning

1.	Input	:	Max : 2Vpp, Input Current: 1mA, Max : 3mA
2.	Data	:	Low level : -0.3V Max: 1.5V, High level : 3.0V Max : Vcc+0.5V
3.	Input	:	Max : 2Vpp, Input Current: 1mA, Max : 3mA
4.	Clock	:	Low level : -0.3V Max: 1.5V, High level : 3.0V Max : Vcc+0.5V
5.	Input	:	Max : 2Vpp, Input Current: 1mA, Max : 3mA
6.	Input	:	Max : 2Vpp, Input Current: 1mA, Max : 3mA
7.	Prog		
8.	Input	:	Max : 2Vpp, Input Current: 1mA, Max: 3mA
9.	Vcc	:	12V
10.	Input	:	Max : 2Vpp, Input Current: 1mA, Max : 3mA
11.	Input	:	Max : 2Vpp, Input Current: 1mA, Max : 3mA

12. Ground
13. Output : 5.5Vpp, Min : 4.5Vpp
14. Output : 5.5Vpp, Min : 4.5Vpp
15. Output : 5.5Vpp, Min : 4.5Vpp
16. Output : 5.5Vpp, Min : 4.5Vpp
17. Output : 5.5Vpp, Min : 4.5Vpp
18. Output : 5.5Vpp, Min : 4.5Vpp
19. Ground
20. Input : Max : 2Vpp, Input Current : 1mA, Max : 3mA

14.11.VPC3230D

14.11.1.General Description

The VPC 323xD is a high-quality, single-chip video front-end, which is targeted for 4:3 and 16:9, 50/60-Hz and 100/120 Hz TV sets. It can be combined with other members of the DIGIT3000 IC family (such as DDP 331x) and/or it can be used with 3rd-party products. The main features of the VPC 323xD are;
– high-performance adaptive 4H comb filter Y/C separator with adjustable vertical peaking
– multi-standard color decoder PAL/NTSC/SECAM including all substandards
– four CVBS, one S-VHS input, one CVBS output
– two RGB/YC $_r$ C $_b$ component inputs, one Fast Blank (FB) input
– integrated high-quality A/D converters and associated clamp and AGC circuits
– multi-standard sync processing
– linear horizontal scaling (0.25 ... 4), as well as non-linear horizontal scaling 'Panorama-vision'
– PAL+ preprocessing
– line-locked clock, data and sync, or 656-output interface
– peaking, contrast, brightness, color saturation and tint for RGB/ YC $_r$ C $_b$ and CVBS/ S-VHS
– high-quality soft mixer controlled by Fast Blank
– PIP processing for four picture sizes (1/4, 1/9, 1/16 or 1/36 of normal size) with 8-bit resolution
– 15 predefined PIP display configurations and expert mode (fully programmable)
– control interface for external field memory
– I^2C-bus interface
– one 20.25-MHz crystal, few external components
– 80-pin PQFP package

14.11.2.Pin Connections and Short Descriptions

NC = not connected
LV = if not used, leave vacant
X = obligatory; connect as described in circuit diagram
SUPPLYA = 4.75...5.25 V, SUPPLYD = 3.15...3.45 V

Pin No. PQFP 80-pin	Pin Name	Type	Connection (if not used)	Short Description
1	B1/CB1IN	IN	VREF	Blue1/Cb1 Analog Component Input
2	G1/Y1IN	IN	VREF	Green1/Y1 Analog Component Input
3	R1/CR1IN	IN	VREF	Read1/Cr1 Analog Component Input
4	B2/CB2IN	IN	VREF	Blue2/Cb2 Analog Component Input
5	G2/Y2IN	IN	VREF	Green2/Y2 Analog Component Input
6	R2/CR2IN	IN	VREF	Read2/Cr2 Analog Component Input
7	ASGF		X	Analog Shield GND_F
8	FFRSTWIN	IN	LV or GND_D	FIFO Reset Write Input
9	V_{SUPCAP}	OUT	X	Digital Decoupling Circuitry Supply Voltage
10	V_{SUPD}	SUPPLYD	X	Supply Voltage, Digital Circuitry
11	GND_D	SUPPLYD	X	Ground, Digital Circuitry
12	GND_{CAP}	OUT	X	Digital Decoupling Circuitry GND
13	SCL	IN/OUT	X	I^2C Bus Clock
14	SDA	IN/OUT	X	I^2C Bus Data
15	RESQ	IN	X	Reset Input, Active Low
16	TEST	IN	GND_D	Test Pin, connect to GND_D
17	VGAV	IN	GND_D	VGAV Input
18	YCOEQ	IN	GND_D	Y/C Output Enable Input, Active Low
19	FFIE	OUT	LV	FIFO Input Enable

20	FFWE	OUT	LV	FIFO Write Enable
21	FFRSTW	OUT	LV	FIFO Reset Write/Read
22	FFRE	OUT	LV	FIFO Read Enable
23	FFOE	OUT	LV	FIFO Output Enable
24	CLK20	IN/OUT	LV	Main Clock output 20.25 MHz
25	GND_{PA}	OUT	X	Pad Decoupling Circuitry GND
26	V_{SUPPA}	OUT	X	Pad Decoupling Circuitry Supply Voltage
27	LLC2	OUT	LV	Double Clock Output
28	LLC1	IN/OUT	LV	Clock Output
29	V_{SUPLLC}	SUPPLYD	X	Supply Voltage, LLC Circuitry
30	GND_{LLC}	SUPPLYD	X	Ground, LLC Circuitry
31	Y7	OUT	GND_Y	Picture Bus Luma (MSB)
32	Y6	OUT	GND_Y	Picture Bus Luma
33	Y5	OUT	GND_Y	Picture Bus Luma
34	Y4	OUT	GND_Y	Picture Bus Luma
35	GND_Y	SUPPLYD	X	Ground, Luma Output Circuitry
36	V_{SUPY}	SUPPLYD	X	Supply Voltage, Luma Output Circuitry
37	Y3	OUT	GND_Y	Picture Bus Luma
38	Y2	OUT	GND_Y	Picture Bus Luma
39	Y1	OUT	GND_Y	Picture Bus Luma
40	Y0	OUT	GND_Y	Picture Bus Luma (LSB)
41	C7	OUT	GND_C	Picture Bus Chroma (MSB)
42	C6	OUT	GND_C	Picture Bus Chroma
43	C5	OUT	GND_C	Picture Bus Chroma
44	C4	OUT	GND_C	Picture Bus Chroma
45	V_{SUPC}	SUPPLYD	X	Supply Voltage, Chroma Output Circuitry
46	GND_C	SUPPLYD	X	Ground, Chroma Output Circuitry
47	C3	OUT	GND_C	Picture Bus Chroma
48	C2	OUT	GND_C	Picture Bus Chroma
49	C1	OUT	GND_C	Picture Bus Chroma
50	C0	OUT	GND_C	Picture Bus Chroma (LSB)
51	GND_{SY}	SUPPLYD	X	Ground Sync Pad Circuitry
52	V_{SUPSY}	SUPPLYD	X	Supply Voltage, Sync Pad Circuitry
53	INTLC	OUT	LV	Interlace Output
54	AVO	OUT	LV	Active Video Output
55	FSY/HC/HSYA	OUT	LV	Front Sync/ Horizontal Clamp Pulse/Front-End Horizontal Sync Output
56	MSY/HS	IN/OUT	LV	Main Sync/Horizontal Sync Pulse
57	VS	OUT	LV	Vertical Sync Pulse
58	FPDAT/VSYA	IN/OUT	LV	Front End/Back-End Data/Front-End Vertical Sync Output
59	V_{STBYY}	SUPPLYA	X	Standby Supply Voltage
60	CLK5	OUT	LV	CCU 5 MHz Clock Output
61	NC	-	LV or GND_D	Not Connected
62	XTAL1	IN	X	Analog Crystal Input
63	XTAL2	OUT	X	Analog Crystal Output
64	ASGF		X	Analog Shield GND_F
65	GND_F	SUPPLYA	X	Ground, Analog Front-End
66	VRT	OUTPUT	X	Reference Voltage Top, Analog
67	I2CSEL	IN	X	I^2C Bus Address Select
68	ISGND	SUPPLYA	X	Signal Ground for Analog Input, connect to GND_F
69	V_{SUPF}	SUPPLYA	X	Supply Voltage, Analog Front-End
70	VOUT	OUT	LV	Analog Video Output
71	CIN	IN	LV	Chroma/Analog Video 5 Input
72	VIN1	IN	VRT	Video 1 Analog Input
73	VIN2	IN	VRT	Video 2 Analog Input
74	VIN3	IN	VRT	Video 3 Analog Input
75	VIN4	IN	VRT	Video 4 Analog Input
76	V_{SUPAI}	SUPPLYA	X	Supply Voltage, Analog Component Inputs Front-End
77	GND_{AI}	SUPPLYA	X	Ground, Analog Component Inputs Front-End
78	VREF	OUTPUT	X	Reference Voltage Top, Analog Component Inputs Front-End
79	FB1IN	IN	VREF	Fast Blank Input
80	AISGND	SUPPLYA	X	Signal Ground for Analog Component Inputs, connect to GND_{AI}

14.12.TDA1308T

14.12.1.General Description

The TDA1308 is an integrated class AB stereo headphone driver contained in an SO8 or a DIP8 plastic package. The device is fabricated in a 1 mm CMOS process and has been primarily developed for portable digital audio applications. It gets its input from two analog audio outputs (DACA_L and DACA_R) of MSP3411G. The gain of the output is adjustable by the feedback resistor between the inputs and outputs.

14.12.2.Features

- Wide temperature range
- No switch ON/OFF clicks
- Excellent power supply ripple rejection
- Low power consumption
- Short-circuit resistant
- High performance
- high signal-to-noise ratio
- High slew rate
- Low distortion
- Large output voltage swing.

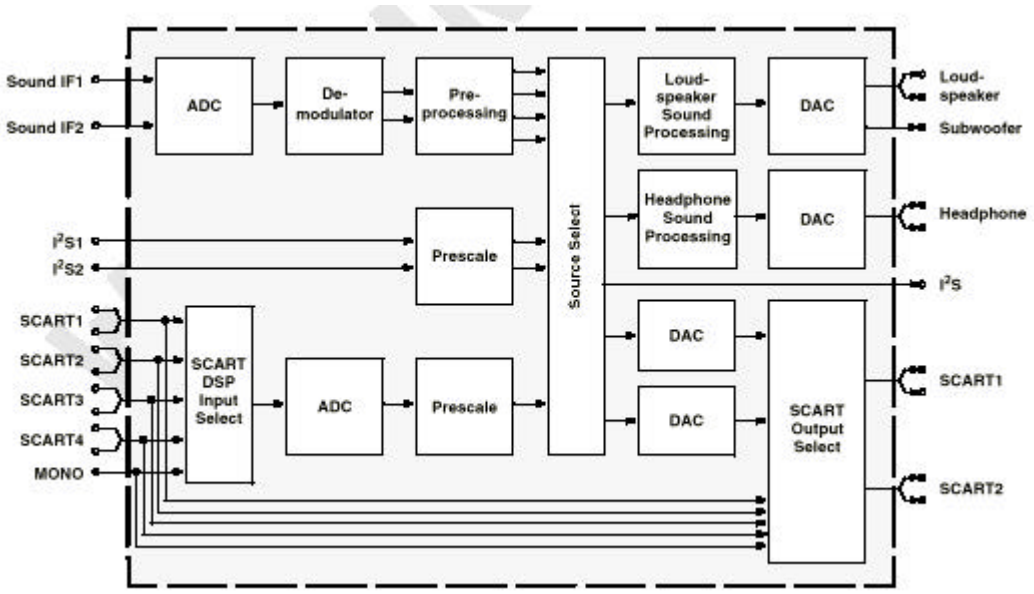
14.12.3.Pinning

SYMBOL	PIN	DESCRIPTION
OUTA	1	Output A
INA(neg)	2	Inverting input A
INA(pos)	3	Non-inverting input A
V_{SS}	4	Negative supply
INB(pos)	5	Non-inverting input B
INB(neg)	6	Inverting input B
OUTB	7	Output B
V_{DD}	8	Positive supply

14.13.MSP34X1G (MSP3411G)

14.13.1.Description

The MSP 34x1G family of single-chip Mullet-standard Sound Processors covers the sound processing of all analog TV-Standards worldwide, as well as the NICAM digital sound standards. The full TV sound processing, starting with analog sound IF signal-in, down to processed analog AF-out, is performed on a single chip. Figure shows a simplified functional block diagram of the MSP34x1G. The MSP34x1G has all functions of the MSP34x0G with the addition of a virtual surround sound feature. Surround sound can be reproduced to a certain extent with two loudspeakers. The MSP34x1G includes our virtualizer algorithm “3D-PANORAMA” which has been approved by the Dolby 1) Laboratories for compliance with the "Virtual Dolby Surround" technology. In addition, the MSP34x1G includes the “PANORAMA” algorithm. These TV sound processing ICs include versions for processing the multi-channel television sound (MTS) signal conforming to the standard recommended by the Broadcast Television Systems Committee (BTSC). The DBX noise reduction, or alternatively, Micronas Noise Reduction (MNR) is performed alignment free. Other processed standards are the Japanese FM-FM multiplex standard (EIA-J) and the FM Stereo Radio standard. Current ICs have to perform adjustment procedures in order to achieve good stereo separation for BTSC and EIA-J. The MSP34x1G has optimum stereo performance without any adjustments. All MSP 34xxG versions are pin and software downward compatible to the MSP 34xxD. MSP34x1G further simplifies controlling software. Standard selection requires a single I^2C transmission only. The MSP34x1G has built-in automatic functions: The IC is able to detect the actual sound standard automatically (Automatic Standard Detection). Furthermore, pilot levels and identification signals can be evaluated internally with subsequent switching between mono/stereo/bilingual; no I^2C interaction is necessary (Automatic Sound Selection).



14.13.2.Features

3D-PANORAMA virtualizer (approved by Dolby Laboratories) with noise generator
PANORAMA virtualizer algorithm
Standard Selection with single I²C transmission
Automatic Standard Detection of terrestrial TV standards/Automatic Carrier Mute function
Automatic Sound Selection (mono/stereo/bilingual), new registers MODUS, STATUS
Two selectable sound IF (SIF) inputs
Interrupt output programmable (indicating status change)
Loudspeaker / Headphone channel with volume, balance, bass, treble, loudness
Loudspeaker channel with MDB (Micronas Dynamic Bass)
AVC: Automatic Volume Correction
Subwoofer output with programmable low-pass and complementary high-pass filter
5-band graphic equalizer for loudspeaker channel
Spatial effect for loudspeaker channel; processing of all deemphasis filtering
Four Stereo SCART (line) inputs, one Mono input; two Stereo SCART outputs
Complete SCART in/out switching matrix
Two I²S inputs; one I²S output
All analog FM-Stereo A2 and satellite standards
All analog Mono sound carriers including AM-SECAM L
Simultaneous demodulation of (very) high-deviation FM-Mono and NICAM
Adaptive deemphasis for satellite (Wegener-Panda, acc. to ASTRA specification)
ASTRA Digital Radio (ADR) together with DRP 3510A
All NICAM standards
Korean FM-Stereo A2 standard

14.13.3.Pin connections

NC = not connected; leave vacant
LV = if not used, leave vacant
X = obligatory; connect as described in circuit diagram
DVSS: if not used, connect to DVSS
AHVSS: connect to AHVSS

Pin No.					Pin Name	Type	Connection (if not used)	Short Description
PLCC 68-pin	PSDIP 64-pin	PSDIP 52-pin	PQFP 80-pin	PLQFP 64-pin				
1	16	14	9	8	ADR_WS	OUT	LV	ADR word strobe
2	-	-	-	-	NC		LV	Not connected
3	15	13	8	7	ADR_DA	OUT	LV	ADR Data Output
4	14	12	7	6	I2S_DA_IN1	IN	LV	I²S1 data input
5	13	11	6	5	I2S_DA_OUT	OUT	LV	I²S data output

6	12	10	5	4	I2S_WS	IN/OUT	LV	I²S word strobe
7	11	9	4	3	I2S_CL	IN/OUT	LV	I²S clock
8	10	8	3	2	I2C_DA	IN/OUT	X	I²C data
9	9	7	2	1	I2C_CL	IN/OUT	X	I²C data
10	8	-	1	64	NC		LV	Not connected
11	7	6	80	63	STANDBYQ	IN	X	Stand-by (low-active)
12	6	5	79	62	ADR_SEL	IN	X	I²C bus address select
13	5	4	78	61	D_CTR_I/O_0	IN/OUT	LV	D_CTR_I/O_0
14	4	3	77	60	D_CTR_I/O_1	IN/OUT	LV	D_CTR_I/O_1
15	3	-	76	59	NC		LV	Not connected
16	2	-	75	58	NC		LV	Not connected
17	-	-	-	-	NC		LV	Not connected
18	1	2	74	57	AUD_CL_OUT	OUT	LV	Audio clock output (18.432 MHz)
19	64	1	73	56	TP		LV	Test pin
20	63	52	72	55	XTAL_OUT	OUT	X	Crystal oscillator
21	62	51	71	54	XTAL_IN	IN	X	Crystal oscillator
22	61	50	70	53	TESTEN	IN	X	Test pin
23	60	49	69	52	ANA_IN2+	IN	AVSS via 56 pF/LV	IF Input 2 (can be left vacant, only if IF input 1 is also not in use)
24	59	48	68	51	ANA_IN-	IN	AVSS via 56 pF/LV	IF common (can be left vacant, only if IF input 1 is also not in use)
25	58	47	67	50	ANA_IN1+	IN	LV	IF input 2
26	57	46	66	49	AVSUP		X	Analog power supply 5v
-	-	-	65	-	AVSUP		X	Analog power supply 5v
-	-	-	64	-	NC		LV	Not connected
-	-	-	63	48	NC		LV	Not connected
27	56	45	62	48	AVSS		X	Analog ground
-	-	-	61	-	AVSS		X	Analog ground
28	55	44	60	47	MONO_IN	IN	LV	Mono input
-	-	-	59	-	NC		LV	Not connected
29	54	43	58	46	VREFTOP		X	Reference voltage IF A/D converter
30	53	42	57	45	SC1_IN_R	IN	LV	SCART 1 input, right
31	52	41	56	44	SC1_IN_L	IN	LV	SCART 1 input, left
32	51	-	55	43	ASG		AHVSS	Analog Shield Ground
33	50	40	54	42	SC2_IN_R	IN	LV	SCART 2 input, right
34	49	39	53	41	SC2_IN_L	IN	LV	SCART 2 input, left
35	48	-	52	40	ASG		AHVSS	Analog Shield Ground
36	47	38	51	39	SC3_IN_R	IN	LV	SCART 3 input, right
37	46	37	50	38	SC3_IN_L	IN	LV	SCART 3 input, left
38	45	-	49	37	ASG		AHVSS	Analog Shield Ground
39	44	-	48	36	SC4_IN_R	IN	LV	SCART 4 input, right
40	43	-	47	35	SC4_IN_L	IN	LV	SCART 4 input, left
41	-	-	46	-	NC		LV or AHVSS	Not connected
42	42	36	45	34	AGNDC		X	Analog reference voltage
43	41	35	44	33	AHVSS		X	Analog ground
-	-	-	43	-	AHVSS		X	Analog ground
-	-	-	42	-	NC		LV	Not connected
-	-	-	41	-	NC		LV	Not connected
44	40	34	40	32	CAPL_M		X	Volume capacitor MAIN
45	39	33	39	31	AHVSUP		X	Analog power supply 8V
46	38	32	38	30	CAPL_A		X	Volume capacitor AUX
47	37	31	37	29	SC1_OUT_L	OUT	LV	SCART output 1, left
48	36	30	36	28	SC1_OUT_R	OUT	LV	SCART output 1, right
49	35	29	35	27	VREF		X	Reference ground 1
50	34	28	34	26	SC2_OUT_L	OUT	LV	SCART output 2, left
51	33	27	33	25	SC2_OUT_R	OUT	LV	SCART output 2, right
52	-	-	32	-	NC		LV	Not connected
53	32	-	31	24	NC		LV	Not connected
54	31	26	30	23	DACM_SUB	OUT	LV	Subwoofer output
55	30	-	29	22	NC		LV	Not connected
56	29	25	28	21	DACM_L	OUT	LV	Loudspeaker out, left
57	28	24	27	20	DACM_R	OUT	LV	Loudspeaker out, right
58	27	23	26	19	VREF2		X	Reference ground 2
59	26	22	25	18	DACA_L	OUT	LV	Headphone out, left
60	25	21	24	17	DACA_R	OUT	LV	Headphone out, right
-	-	-	23	-	NC		LV	Not connected
-	-	-	22	-	NC		LV	Not connected
61	24	20	21	16	RESETQ	IN	X	Power-on-reset
62	23	-	20	15	NC		LV	Not connected

63	22	-	19	14	NC		LV	Not connected
64	21	19	18	13	NC		LV	Not connected
65	20	18	17	12	I2S_DA_IN2	IN	LV	I²S2-data input
66	19	17	16	11	DVSS		X	Digital ground
-	-	-	15	-	DVSS		X	Digital ground
-	-	-	14	-	DVSS		X	Digital ground
67	18	16	13	10	DVSUP		X	Digital power supply 5V
-	-	-	12	-	DVSUP		X	Digital power supply 5V
-	-	-	11	-	DVSUP		X	Digital power supply 5V
68	17	15	10	9	ADR_CL	OUT	LV	ADR clock

14.14.TL431

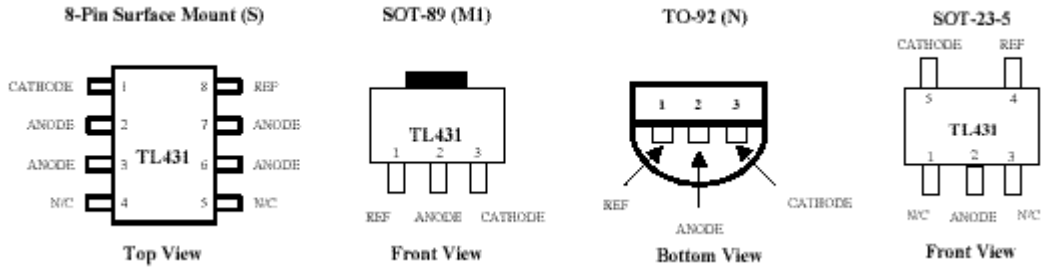
14.14.1.Description

The TL431 is a 3-terminal adjustable shunt voltage regulator providing a highly accurate 1 % band gap reference. TL431 acts as an open-loop error amplifier with a 2.5V temperature compensation reference. The TL431 thermal stability, wide operating current (150mA) and temperature range (0.to 105.makes it suitable for all variety of application that are looking for a low cost solution with high performance. The output voltage may be adjusted to any value between VREF and 36 volts with two external resistors. The TL431 is operating in full industrial temperature range of 0°C to 105°C. The TL431 is available in TO-92, SO-8, SOT-89 and SOT23-5 packages.

14.14.2.Features

• Trimmed Band gap to 1%
• Wide Operating Current 1mA to 150mA
• Extended Temperature Range 0. °C to 105.°C
• Low Temperature Coefficient 30 ppm /°C
• Offered in TO-92, SOIC, SOT-89, SOT-23-5
• Improved Replacement in Performance for TL431
• Low Cost Solution

14.14.3.Pin Configurations



14.15.TDA9885/86

14.15.1.Introduction

The TDA9885 is an alignment-free single standard (without positive modulation) vision and sound IF signal PLL. The TDA9886 is an alignment-free multi standard (PAL, SECAM and NTSC) vision and sound IF signal PLL. Both devices can be used for TV, VTR, PC and set-top box applications.

14.15.2.Features

• 5 V supply voltage
• Gain controlled wide-band Vision Intermediate Frequency (VIF) amplifier (AC-coupled)
• Multistandard true synchronous demodulation with active carrier regeneration (very linear demodulation, good intermodulation figures, reduced harmonics, excellent pulse response)
• Gated phase detector for L/L accent standard
• Fully integrated VIF Voltage Controlled Oscillator (VCO), alignment-free; frequencies switchable for all negative and positive modulated standards via I²C-bus
• Digital acquisition help, VIF frequencies of 33.4, 33.9, 38.0, 38.9, 45.75 and 58.75 MHz

• 4 MHz reference frequency input [signal from Phase-Locked Loop (PLL) tuning system] or operating as crystal oscillator
• VIF Automatic Gain Control (AGC) detector for gain control, operating as peak sync detector for negative modulated signals and as a peak white detector for positive modulated signals
• Precise fully digital Automatic Frequency Control (AFC) detector with 4-bit digital-to-analog converter; AFC bits via I²C-bus readable
• Take Over Point (TOP) adjustable via I²C-bus or alternatively with potentiometer
• Fully integrated sound carrier trap for 4.5, 5.5, 6.0 and 6.5 MHz, controlled by FM-PLL oscillator
• Sound IF (SIF) input for single reference Quasi Split Sound (QSS) mode (PLL controlled)
• SIF AGC for gain controlled SIF amplifier; single reference QSS mixer able to operate in high performance single reference QSS mode and in intercarrier mode, switchable via I²C-bus
• AM demodulator without extra reference circuit
• Alignment-free selective FM-PLL demodulator with high linearity and low noise
• I²C-bus control for all functions
• I²C-bus transceiver with pin programmable Module Address (MAD).

14.15.3.Pin Configurations

Symbol	Pin	Description
VIF1	1	VIF differential input 1
VIF2	2	VIF differential input 2
OP1	3	output 1 (open-collector)
FMPLL	4	FM-PLL for loop filter
DEEM	5	de-emphasis output for capacitor
AFD	6	AF decoupling input for capacitor
DGND	7	digital ground
AUD	8	audio output
TOP	9	tuner AGC TakeOver Point (TOP)
SDA	10	I²C-bus data input/output
SCL	11	I²C-bus clock input
SIOMAD	12	sound intercarrier output and MAD select
n.c	13	not connected
TAGC	14	tuner AGC output
REF	15	4 MHz crystal or reference input
VAGC	16	VIF-AGC for capacitor (Not connected for TDA9885.)
CVBS	17	video output
AGND	18	analog ground
VPLL	19	VIF-PLL for loop filter
V_P	20	supply voltage (+5 V)
AFC	21	output
OP2	22	output 2 (open-collector)
SIF1	23	differential input 1
SIF2	24	differential input 2

14.16.LM7808

14.16.1.Description

The L7800 series of three-terminal positive regulators is available in TO-220 TO-220FP TO-3 and D 2 PAK packages and several fixed output voltages, making it useful in a wide range of applications. These regulators can provide local on-card regulation, eliminating the distribution problems associated with single point regulation. Each type employs internal current limiting, thermal shutdown and safe area protection, making it essentially indestructible. If adequate heat sinking is provided, they can deliver over 1A output current. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

14.16.2.Features

Output Current Up To 1.5 A
Output Voltages of 5; 5.2; 6; 8; 8.5; 9; 12; 15; 18; 24V
Thermal Over load protection
Short Circuit Protection
Output Transition SOA Protection

14.17.TDA8177F

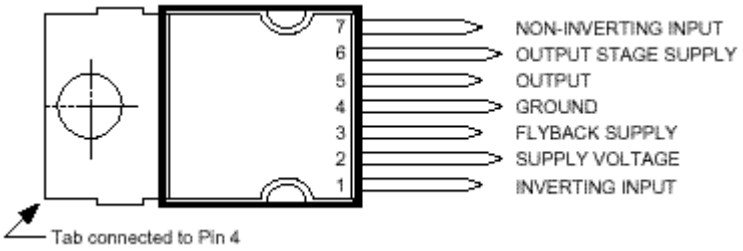
14.17.1.Description

Designed for monitors and high performance TVs, the TDA8177F vertical deflection booster can handle flyback voltage up to 70V. More than this it is possible to have a flyback voltage, which is more than the double of the supply (Pin 2). This allows to decrease the power consumption or to decrease the flyback time for a given supply voltage. The TDA8177F operates with supplies up to 35V and provides up to 3APP output current to drive the yoke.

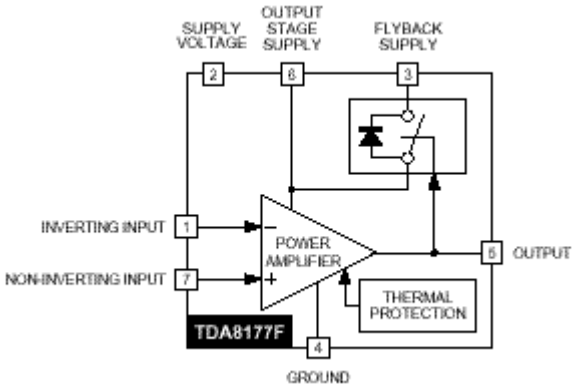
14.17.2.Features

Power Amplifier
Thermal Protection
Output Current Up To 3.0APP
Flyback Voltage Up To 70V (on Pin 5)
Suitable For Dc Coupling Application
External Flyback Supply

14.17.3.Pin connections



14.17.4.Block Diagram



14.18.LM1086

14.18.1.Description

The LM1086 is a series of low dropout positive voltage regulators with a maximum dropout of 1.5V at 1.5A of load current. It has the same pin-out as National Semiconductor's industry standard LM317. The LM1086 is available in an adjustable version, which can set the output voltage with only two external resistors. It is also available in five fixed voltages: 2.5V, 2.85V, 3.3V, 3.45V and 5.0V. The fixed versions integrate the adjust resistors. The LM1086 circuit includes a zener trimmed band-gap reference, current limiting and thermal shutdown.

14.18.2.Features

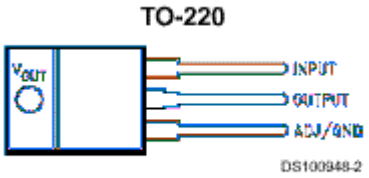
Available in 2.5V, 2.85V, 3.3V, 3.45V, 5V and Adjustable Versions
Current Limiting and Thermal Protection
Output Current 1.5A

Line Regulation 0.015% (typical)
Load Regulation 0.1% (typical)

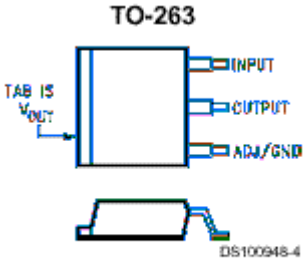
14.18.3.Applications

SCSI-2 Active Terminator
High Efficiency Linear Regulators
Battery Charger
Post Regulation for Switching Supplies
Constant Current Regulator
Microprocessor Supply

14.18.4.Connection Diagrams



Top View



Top View

14.19.MC44608

14.19.1.Description

The MC44608 is a high performance voltage mode controller designed for off–line converters. This high voltage circuit that integrates the start–up current source and the oscillator capacitor, requires few external components while offering a high flexibility and reliability. The device also features a very high efficiency stand–by management consisting of an effective Pulsed Mode operation. This technique enables the reduction of the stand–by power consumption to approximately 1W while delivering 300mW in a 150W SMPS.

• Integrated Start–Up Current Source
• Lossless Off–Line Start–Up
• Direct Off–Line Operation
• Fast Start–Up

14.19.2.General Features

• Flexibility
• Duty Cycle Control
• Under voltage Lockout with Hysteresis
• On Chip Oscillator Switching Frequency 40, or 75kHz
• Secondary Control with Few External Components

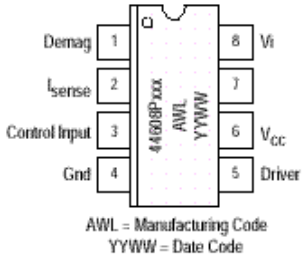
Protections

• Maximum Duty Cycle Limitation
• Cycle by Cycle Current Limitation
• Demagnetization (Zero Current Detection) Protection
• “Over VCC Protection” Against Open Loop
• Programmable Low Inertia Over Voltage Protection Against Open Loop
• Internal Thermal Protection

GreenLine™ Controller

• Pulsed Mode Techniques for a Very High Efficiency Low Power Mode
• Lossless Startup
• Low dV/dT for Low EMI Radiations

14.19.3.Pin Connections



14.19.4.Pin Function description

Pin	Name	Description
1	Demag	The Demag pin offers 3 different functions: Zero voltage crossing detection (50mV), 24mA current detection and 120mA current detection. The 24mA level is used to detect the secondary reconfiguration status and the 120mA level to detect an Over Voltage status called Quick OVP.
2	ISENSE	The Current Sense pin senses the voltage developed on the series resistor inserted in the source of the power MOSFET. When I sense reaches 1V, the Driver output (pin 5) is disabled. This is known as the Over Current Protection function. A 200mA current source is flowing out of the pin 3 during the start–up phase and during the switching phase in case of the Pulsed Mode of operation. A resistor can be inserted between the sense resistor and the pin 3; thus a programmable peak current detection can be performed during the SMPS stand–by mode.
3	Control Input	A feedback current from the secondary side of the SMPS via the opto–coupler is injected into this pin. A resistor can be connected between this pin and GND to allow the programming of the Burst duty cycle during the Stand–by mode.
4	Ground	This pin is the ground of the primary side of the SMPS.
5	Driver	The current and slew rate capability of this pin are suited to drive Power MOSFETs.
6	VCC	This pin is the positive supply of the IC. The driver output gets disabled when the voltage becomes higher than 15V and the operating range is between 6.6V and 13V. An intermediate voltage level of 10V creates a disabling condition called Latched Off phase.
7		This pin is to provide isolation between the Vi pin 8 and the VCC pin 6.
8	Vi	This pin can be directly connected to a 500V voltage source for start–up function of the IC. During the Start–up phase a 9 mA current source is internally delivered to the VCC pin 6 allowing a rapid charge of the VCC capacitor. As soon as the IC starts–up, this current source is disabled.

14.20.TCET1102G

14.20.1.Description

The TCET110/ TCET2100/ TCET4100 consists of a phototransistor optically coupled to a gallium arsenide infrared-emitting diode in a 4-lead up to 16-lead plastic dual inline package. The elements are mounted on one lead frame using a **coplanar techniqu**e, providing a fixed distance between input and output for highest safety requirements.

14.20.2.Applications

Circuits for safe protective separation against electrical shock according to safety class II (reinforced isolation):
For appl. class I – IV at mains voltage =300 V
For appl. class I – III at mains voltage =600 V
According to VDE 0884, table 2, suitable for: **Switch-mode power supplies, line receiver, computer peripheral interface, microprocessor system interface.**

14.20.3.Features

VDE 0884 related features:
Rated impulse voltage (transient overvoltage) V_{IOTM} = 8 kV peak
Isolation test voltage (partial discharge test voltage) V_{pd} = 1.6 kV
Rated isolation voltage (RMS includes DC) V_{IOWM} = 600 V $_{RMS}$ (848 V peak)
Rated recurring peak voltage (repetitive) V_{IORM} = 600 V $_{RMS}$

General features:
CTR offered in 9 groups
Isolation materials according to UL94-VO
Pollution degree 2 (DIN/VDE 0110 / resp. IEC 664)
Climatic classification 55/100/21 (IEC 68 part 1)
Special construction: Therefore, extra low coupling capacity of typical 0.2pF, high **C**ommon **M**ode **R**ejection
Low temperature coefficient of CTR
G = Leadform 10.16 mm; provides creepage distance > 8 mm, for TCET2100/ TCET4100 optional; suffix letter 'G' is not marked on the optocoupler
Coupling System U

14.21.TDA7480L

14.21.1.Description

The TDA7480L is an audio class-D amplifier assembled in Power DIP package specially de-signed for high efficiency applications mainly for TV and Home Stereo sets.

14.21.2.Features

10W Output Power: R_L = 8Ω/4Ω; THD = 10%
High Frequency
No Heatsink
Split Supply
Overvoltage Protection
St-By And Mute Features
Short Circuit Protection
Thermal Overload Protection

14.21.3.Pin Functions

Number	Name	Function
1	$-V_{CC}$	NEGATIVE SUPPLY.
2	$-V_{CC}$	NEGATIVE SUPPLY.
3	$-V_{CC}$	NEGATIVE SUPPLY.
4	OUT	PWM OUTPUT
5	BOOTDIODE	BOOTSTRAP DIODE ANODE
6	BOOT	BOOTSTRAP CAPACITOR
7	NC	NOT CONNECTED
8	FEEDCAP	FEEDBACK INTEGRATING CAPACITANCE
9	FREQUENCY	SETTING FREQUENCY RESISTOR
10	SGN-GND	SIGNAL GROUND
11	IN	INPUT
12	ST-BY-MUTE	ST-BY/ MUTE CONTROL PIN
13	NC	NOT CONNECTED
14	$+V_{CC}$ SIGN	POSITIVE SIGNAL SUPPLY
15	V_{REG}	10V INTERNAL REGULATOR
16	$+V_{CC}$ POW	POSITIVE POWER SUPPLY
17	$-V_{CC}$	NEGATIVE SUPPLY (TO BE CONNECTED TO PIN 16 VIA C5)
18	$-V_{CC}$	NEGATIVE SUPPLY
19	$-V_{CC}$	NEGATIVE SUPPLY
20	$-V_{CC}$	NEGATIVE SUPPLY

14.22.SAA3010T

14.22.1.Description

The SAA3010 is intended as a general purpose (RC-5) infrared remote control system for use where a low voltage supply and a large debounce time are expected. The device can generate 2048 different commands and utilizes a keyboard with a single pole switch for each key. The commands are arranged so that 32 systems can be addressed, each system containing 64 different commands. The circuit response to legal (one key pressed at a time) and illegal (more than one key pressed at a time) keyboard operation is specified in the section "Keyboard operation".

14.22.2.Features

Low voltage requirement
Biphase transmission technique
Single pin oscillator
Test mode facility

14.22.3.Pinning

Pin	Mnemonic	Function
1	X7 (IPU)	sense input from key matrix
2	SSM (I)	sense mode selection input
3	Z0-Z3 (IPU)	sense inputs from key matrix
7	MDATA (OP3)	generated output data modulated with 1/12 the oscillator frequency at a 25% duty factor
8	DATA (OP3)	generated output information
9-13	DR7-DR3 (ODN)	Scan drivers
14	VSS	Ground (0V)
15-17	DR-2-DR0 (ODN)	Scan drivers
18	OSC (I)	Oscillator input
19	TP2 (I)	test point 2
20	TP1 (I)	Test point 1
21-27	X0-X6 (IPU)	Sense inputs from key matrix
28	VDD(I)	Voltage supply

Note:
(I): Input,
(IPU): input with p-channel pull-up transistor,
(ODN): output with open drain n-channel transistor
(OD3): output 3-state

15.AK52 CHASSIS MANUAL ADJUSTMENTS PROCEDURE

15.1.PRELIMINARY

Before starting with the alignment procedure, make sure that all the potentiometers on the chassis and also screen and focus pots are in the medium position.

15.2.SYSTEM VOLTAGE ADJUSTMENTS

Inputs AC power (220V 50Hz)
PAL B/G test pattern via RF
(PAL I test pattern for PAL I TV's, SECAM D/K pattern, SECAM L/L'/K' TVs.)
Outputs Digital voltmeter to anode of D110.
Display System voltage
Action Apply power. Check that the stand-by Led lights.
Select TV mode and tune to the applied test pattern via local test keyboard.
Chassis should start normally.
Adjust all analog controls (volume, bass, treble, brightness, contrast, colour) to minimum settings.
Adjust VR127 according to the following different type of CRTs.

SYSTEM VOLTAGE	TYPE OF CRT
135V±0.5V	PHILIPS A66EAK552X54
135V±0.5V	PHILIPS A66EAK071X54
135V±0.5V	VIDEOCOLOR A66ECY13X12
135V±0.5V	PHILIPS W66ESF002X44

15.3.AFC ADJUSTMENTS

AFC is automatically adjusted from software , when f (IF) is selected 38.9MHz for negative modulation and 33.9MHz for positive modulation from the service menu.

15.4.FOCUS ADJUSTMENTS

Inputs AC power
PAL B/G test pattern via RF input.
Outputs Picture tube drive.
Display Picture
Action Select TV mode and tune to the signal.
Adjust focus potantiometer (the upper pot on the rear side of the FBT transformer) for optimum focusing drive.

15.5.SCREEN ADJUSTMENTS

Inputs AC power
PAL B/G Colour Bar test pattern via RF
Outputs 1/100 Oscilloscope probe to RGB cathodes on CRT baseboard.
NOTE: Ground pin of probe will be connected to 1st pin (GND) of the CRT socket.
Display RGB ratio
Action Select PAL B/G Colour bar pattern using the local test keyboard and the user remote control unit.
Adjust all control functions (brightness, colour and contrast) to minimum settings.
Measure the most sensitive cathode
Adjust the screen potentiometer (lower pot on the rear side of FBT transformer) until cathode voltage becomes 150V.

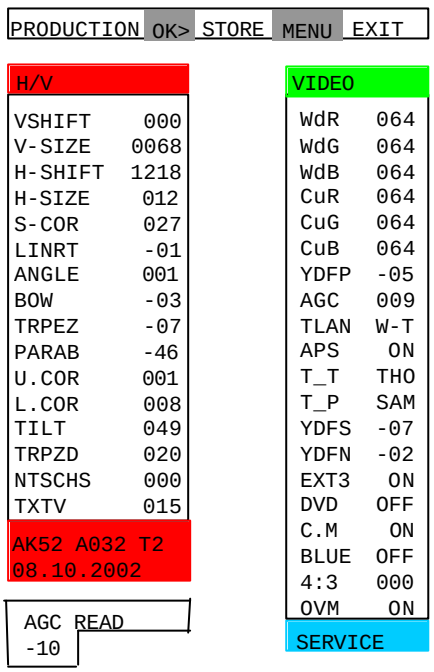
15.6.IF ADJUSTMENT FOR L' MODE

AFC is automatically adjusted from software , when f (IF) is selected 33.9MHz for positive modulation (SECAM L') from the service menu.

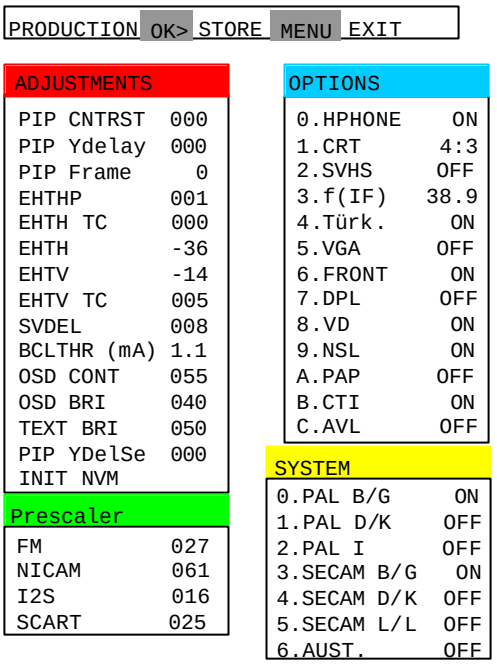
16.AK52 CHASSIS PRODUCTION SERVICE MODE ADJUSTMENTS

16.1.PRELIMINARY

All system, geometry and white balance alignments are performed in production service mode. Before starting the production mode alignments, make sure that all manual adjustments are done correctly. To start production mode alignments enter the MAIN MENU and then press the digits 1, 6, 7 and 5 respectively. The following first menu appears on the screen. Production mode values will appear on the screen.



First page



Second Page

SERVICE MENU

Production mode groups will be displayed with different colours of headlines, so in order to access a production alignment group press the colour button of the related group on the remote control transmitter.

- RED BUTTON is pressed to access H/V menu.
- GREEN BUTTON is pressed to access VIDEO adjust menu.
- BLUE BUTTON is pressed to go to the next page of the service menu.
- YELLOW BUTTON is used to adjust system parameters on the second page of the service menu.

After selecting one of the production service mode groups, you can access its items by pressing ? /? buttons. Selected parameter will be highlighted. Inorder to change the selected parameter, use ? / ? buttons. Inorder to switch between other group of items press the colour key of this groups headline.
To store the settings press OK button. To exit the service menu press MENU button.
Entire service menu parameters of AK52 CHASSIS are listed below.

16.2.H/V (HORIZONTAL AND VERTICAL GEOMETRY ALIGNMENTS)

Switch the program to crosshatch test pattern. Press RED button to access this group of item. Select the parameter by pressing up/down buttons. Adjust the parameter by pressing left/right buttons. Store the settings by pressing OK button. Switch the another parameter group by pressing the colour button of the related coloured headline of that group. Exit production mode by pressing the MENU button on the remote control.

V-SHIFT

Change Vertical Shift by pressing Left/Right buttons till the test pattern is vertically centered. Horizontal line at the center of the test pattern is in equal distance both to upper and lower side of the picture tube. Check and readjust V-SHIFT item if the adjustment becomes improper after some other geometric adjustments are done.

Min. Value: -128
Max. Value: 127

Recommended Value: 000

V-SIZE

Change Vertical Size by pressing Left/Right buttons till horizontal black lines on both the upper and lower part of the test pattern become very close to the upper and lower horizontal sides of picture tube and nearly about to disappear. Check and readjust V-SIZE item if the adjustment becomes improper after some other geometric adjustments are done.

Min. Value: -128
Max. Value: 127
Recommended Value: 068

H-SHIFT

Change Horizontal Shift by pressing Left/Right buttons till the the test pattern is horizontally in equal distance both to right and left sides of the picture tube. Check and readjust H-SHIFT item if the adjustment becomes improper after some other geometric adjustments are done.

Min. Value: 0000
Max. Value: 1295
Recommended Value: 1218

H-SIZE

Change Horizontal Size by pressing Left/Right buttons till no under-scan condition will happen, i.e. no white bars on the left and right side of the test pattern will be visible nor picture will be so wide. Check and readjust H-SIZE item if the adjustment becomes improper after some other geometric adjustments are done.

Min. Value: -128
Max. Value: 127
Recommended Value: 012

S-COR

Change S-Correction by pressing Left/Right buttons till the size of squares on both the upper and lower part of test pattern become equal to the squares laying on the vertical center of the test pattern. Check and readjust S-COR item if the adjustment becomes improper after some other geometric adjustments are done.

Min. Value: -128
Max. Value: 127
Recommended Value: 027

LINRT

Change Linearity by pressing Left/Right buttons till all the size of squares of the test pattern become in equal size from the top of the screen to its bottom of the whole screen. Check and readjust LINRT item if the adjustment becomes improper after some other geometric adjustments are done. (especially after than S-COR adjustment)

Min. Value: -128
Max. Value: 127
Recommended Value: -01

ANGLE

Change Angle by pressing Left/Right buttons till the vertical lines of the crosshatch pattern become completely perpendicular to horizontal lines without any angle of vertical deviation. Check and readjust ANGLE item if the adjustment becomes improper after some other geometric adjustments are done.

Min. Value: -128
Max. Value: 127
Recommended Value: 001

BOW

Change Bow by pressing Left/Right buttons till the vertical lines especially ones close to the left and right sides will of equal and symmetrical bending, i.e. they together will neither be towards left side nor right side. Check and readjust BOW item if the adjustment becomes improper after some other geometric adjustments are done.

Min. Value: -128

Max. Value: 127
Recommended Value: -03

TRPEZ
Change Trapezium by pressing Left/Right buttons till vertical lines, especially lines at the sides of the picture frame became parallel to the both sides of picture tube as close as possible. Check and readjust TRPEZ item if the adjustment becomes improper after some other geometric adjustments are done.
Min. Value: -128
Max. Value: 127
Recommended Value: -07

PARAB
Change Parabol by pressing Left/Right buttons till vertical lines close to the both sides of the picture frame become parallel to vertical sides of picture tube without any bending to left or to right side of the screen. Check and readjust PARAB item if the adjustment becomes improper after some other geometric adjustments are done.
Min. Value: -128
Max. Value: 127
Recommended Value: -46

U.COR
Change Upper Correction by pressing Left/Right buttons till vertical lines at the upper corners of the picture frame become vertical and parallel to vertical corner sides of picture tube. Check and readjust U.COR item if the adjustment becomes improper after some other geometric adjustments are done.
Min. Value: -128
Max. Value: 127
Recommended Value: 001

L.COR
Change Lower Correction by pressing Left/Right buttons till vertical lines at the lower corners of the picture frame become vertical and parallel to vertical corner sides of picture tube. Check and readjust L.COR item if the adjustment becomes improper after some other geometric adjustments are done.
Min. Value: -128
Max. Value: 127
Recommended Value: 008

TILT
This adjustment only works when the TV has rotation option. Change TILT by pressing Left/Right buttons to rotate the complete raster clock-wise and counter clock-wise depending on the CRT. Check and readjust TRPEZ item if the adjustment becomes improper after some other geometric adjustments are done.
Min. Value: 000
Max. Value: 063
Recommended Value: 049

TRPZD
Not used for this model.

NTSCHS
Change NTSC horizontal size by pressing Left/Right buttons to adjust till no under-scan condition will happen, i.e. no white bars on the left and right side of the NTSC test pattern will be visible nor picture will be so wide. Check and readjust TRPEZ item if the adjustment becomes improper after some other geometric adjustments are done.
Min. Value: 000
Max. Value: 010
Recommended Value: 000

TXTV
Change TXTV by pressing Left/Right buttons to adjust the proper vertical size of Teletext screen. Check and readjust TRPEZ item if the adjustment becomes improper after some other geometric adjustments are done.

Min. Value:	000
Max. Value:	040
Recommended Value:	015

16.3.VIDEO ALIGNMENTS

Switch the program to colour bar test pattern. Press GREEN button to access this group of item. Select the parameter by pressing up/down buttons. Adjust the parameter by pressing left/right buttons. Store the settings by pressing OK button.

WdR, WdG, WdB: WHITE BALANCE ADJUSTMENT

Apply WHITE test pattern via RF. Adjust all analog functions to medium level and set WdR to 86, WdG to 84, WdB to 80, if needed. Use colour analyser and monitor the colour temperature (X,Y) on colour analyser. Select WdR and WdB by pressing up/down buttons and change the values by Left/Right buttons till the following values are read:
X=285±10
Y=293±10 on the colour analyser.

CuR, CuG, CuB

Set the values of these items as 64 (constant).

YDFP

Enter a PAL B/G colour and black-white bar test pattern via RF. Adjust Y-Delay for PAL till the colour transients on the colour bar of the pattern become as sharper and colours between transients do not mix with each other as possible.

Min. Value:	-07
Max. Value:	001
Recommended Value:	-05

AGC

Apply PAL BG signal, VHF-3 Channel-12 and 60dBuV signal level. Adjust AGC (Automatic Gain Control) item by pressing Left/Right buttons till the voltage at AGC point (pin1 of the tuner) becomes 3.0 volts.

Min. Value:	000
Max. Value:	031
Recommended Value:	016

TLAN

Text language is set. Options are W-T, W-E, W, E. W-T will be selected.

APS

The option of APS (Automatic Program Searching) item are ON and OFF. In order to active APS installation procedure when TV is turned for the very first time, select ON. Inorder to start TV without APS installation procedure, select OFF.

T_T

This item is used for the Tuner selection. The options are SAM for SAMSUNG, THO for THOMSON, SIE for SIEMENS, MK2 and MK3 for PHILIPS MP2/MP3, ALP for ALPS and TEC for Tecnisat. Select THO.

T_P

This item is also used for the Tuner selection. The options are MK2, SAM, THO, TEM. MK2 for PHILIPS, SAM for SAMSUNG, THO for THOMSON and TEM for TEMIC. Select SAM.

YDFS

Enter a SECAM B/G colour and black-white bar test pattern via RF. Adjust Y-Delay SECAM till the colour transients on the colour bar of the pattern become as sharper and colours between transients do not mix with each other as possible.

Min. Value:	-07
Max. Value:	001
Recommended Value:	-07

YDFN
Enter an NTSC colour and black-white bar test pattern via RF. Adjust Y-Delay NTSC till the colour transients on the colour bar of the pattern become as sharper and colours between transients do not mix with each other as possible.

Min. Value:	-07
Max. Value:	001
Recommended Value:	-02

EXT3
Select ON.

DVD
Select OFF.

C.M
Select ON.

BLUE
Select OFF.

4:3
Set to 0.

OVM
Select ON.

16.4.SERVICE ALIGNMENTS

IMPORTANT: There will no adjustments in this service mode during production mode alignments.
Press BLUE colour button on the remote control when Production mode is active. Press the colour button of the related item group headline colour. Press up/down buttons to select the item of group. Press Left/Right button to alter the value of the item. Press OK button to store the selected value and MENU button to exit the service alignments mode.

ADJUSTMENTS GROUP
Press RED button in order to access this group of items.

PIP CNTRST	: Level of the PIP picture
PIP Ydelay	: Luma delay of the PIP picture
PIP Frame	: Colour selection of the PIP frame (edges of the PIP)
EHTHP	: EHT compensation coefficient for horizontal phase
EHTH TC	: EHT time constant for horizontal phase compensation
EHTH	: EHT compensation coefficient for horizontal amplitude
EHTV	: EHT compensation coefficient for vertical amplitude
EHTV TC	: EHT time constant for control of vertical and horizontal amplitude EHT compensation
SVDEL	: Delay adjustment for scan velocity modulation
BCLTHR (mA)	: Beam current applied to the CRT
OSD CONT	: Contrast level of OSD
OSD BRI	: Brightness level of OSD
TEXT BRI	: Brightness level of text
PIP YDelSe	: Y-Delay adjustment for pin-in-picture option
INIT NVM	: Press to initiate the NVM

PRESCALER GROUP
Press GREEN button in order to access this group of items.

FM	: This adjustment is to determine the pre-amplifier gain of MSP for German stereo Set to 27.
NICAM	: This adjustment is to determine the pre-amplifier gain of MSP for Nicam Set to 61.
I2S	: Not used.
SCART	: This adjustment is to determine the pre-amplifier gain of MSP for Scart audio inputs Set to 25.

OPTIONS GROUP

Press BLUE button in order to access this group of items.

0.HPHONE : ON/OFF
1.CRT : 4:3 / 16:9
2.SVHS : ON/OFF
3.f(IF) : always set to 38.9
4.Türk. : Turkish menu ON/OFF
5.VGA : ON/OFF
6.FRONT : Front AV ON/OFF
7.DPL : ON/OFF
8.VD : ON/OFF
9.NSL : ON/OFF
A.PAP : ON/OFF
B.CTI : ON/OFF
C.AVL : ON/OFF

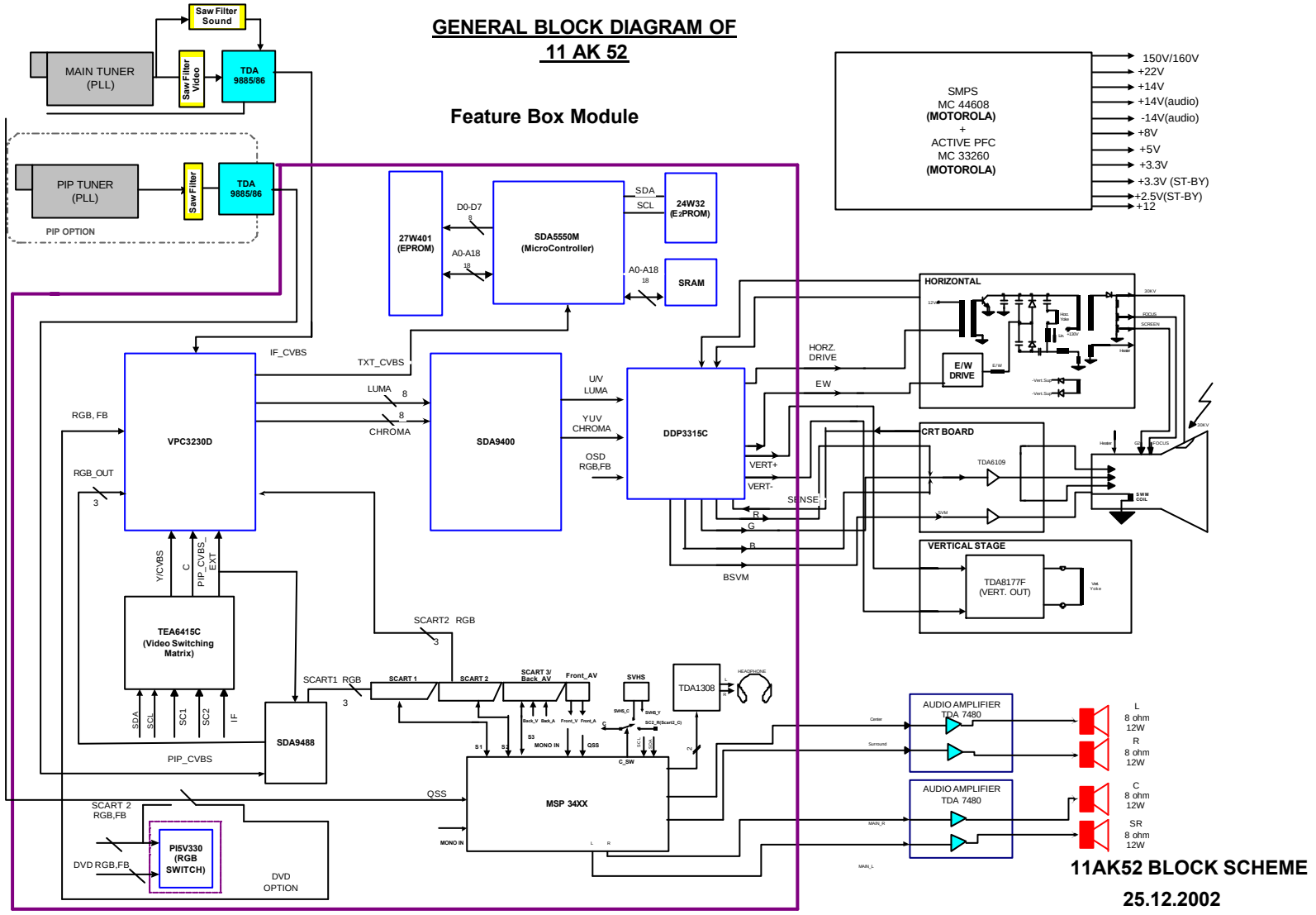
SYSTEM GROUP

Press YELLOW button in order to access this group of items.

0.PAL B/G : ON/OFF
1.PAL D/K : ON/OFF
2.PAL I : ON/OFF
3.SECAM B/G : ON/OFF
4.SECAM D/K : ON/OFF
5.SECAM L/L' : ON/OFF
6.AUST. : ON/OFF

NOTE: Settings values in Service menu are given for 28" 4:3 THOMSON (A66EHJ13X12) tube in this manual.

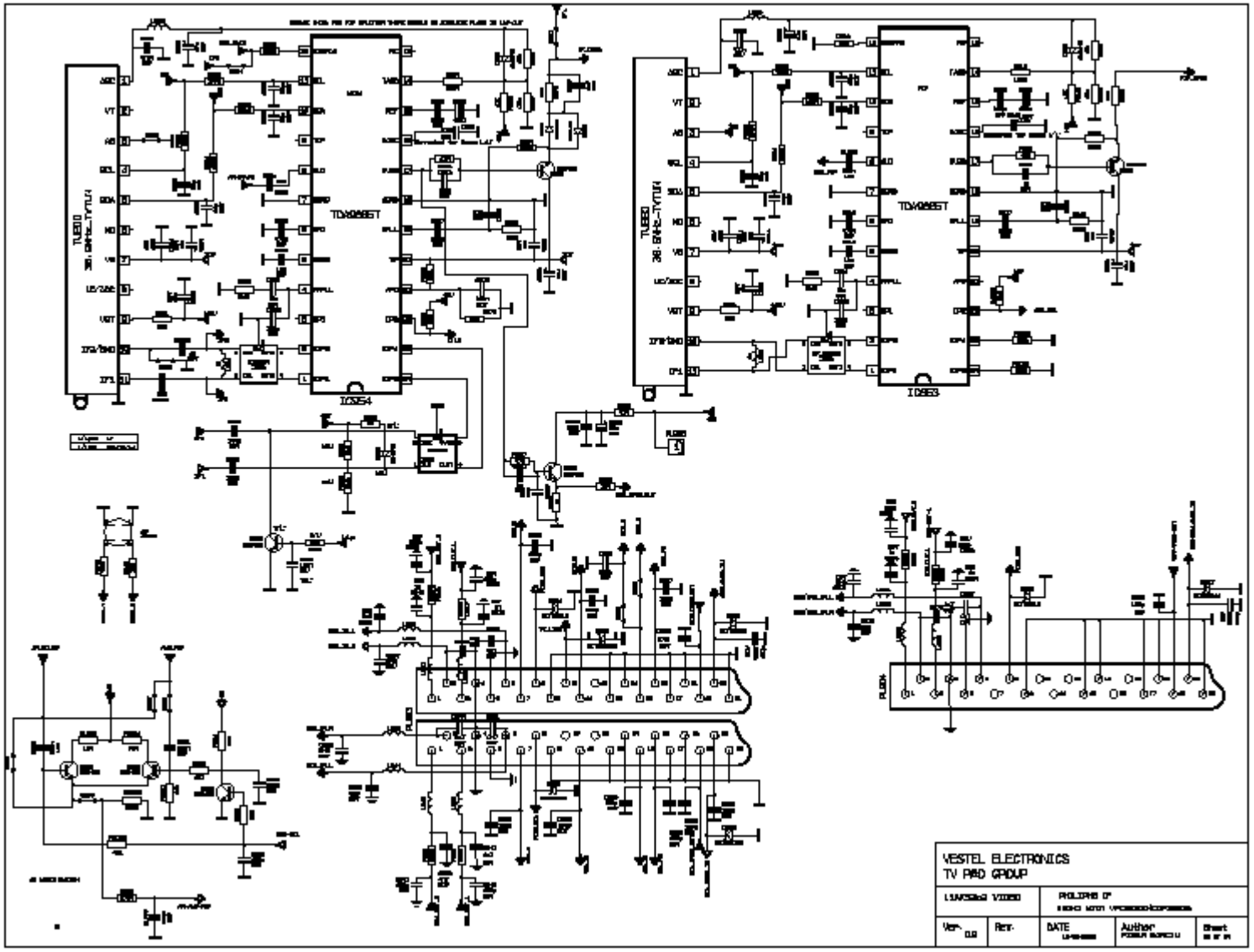
17.BLOCK DIAGRAM



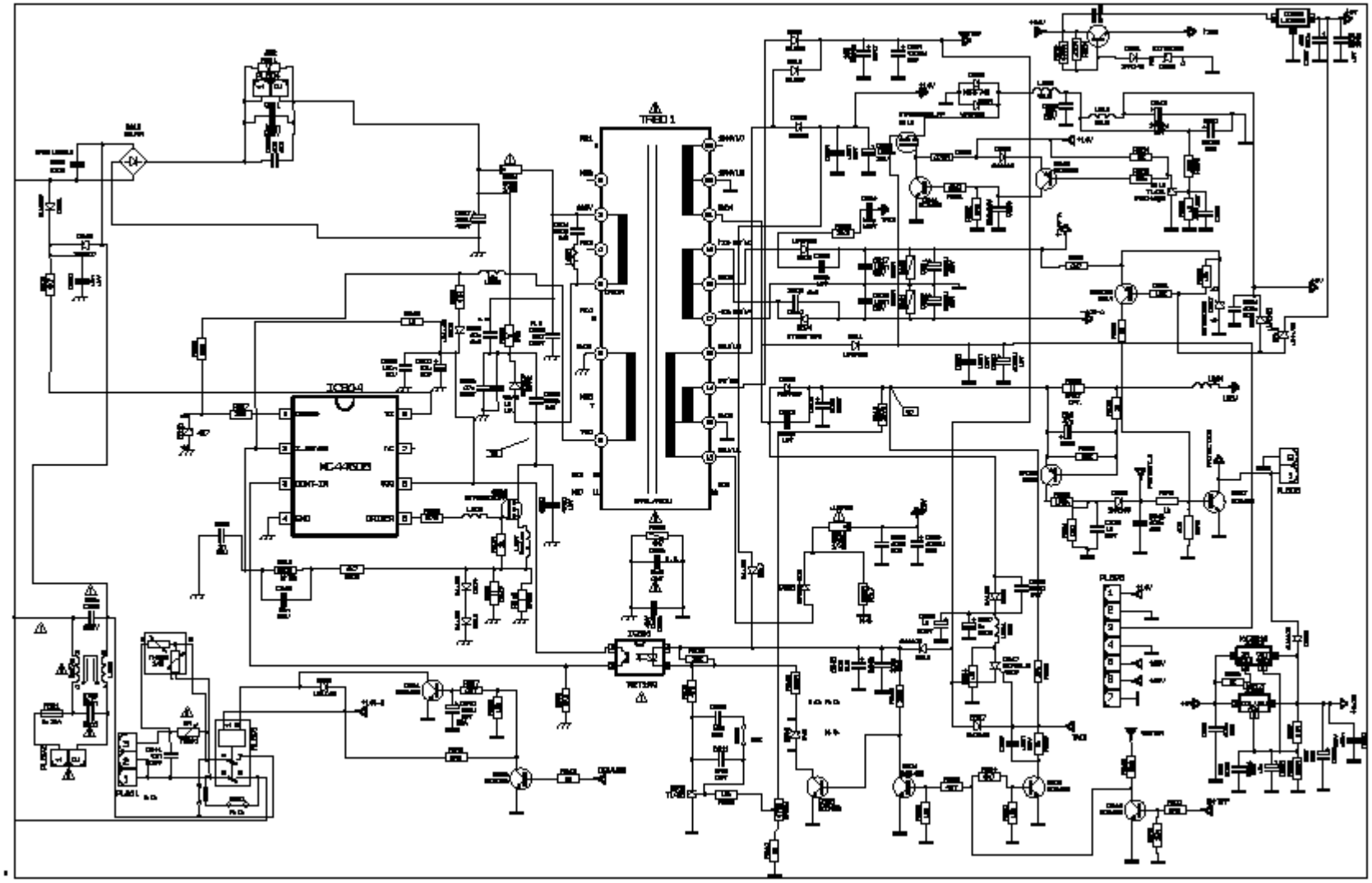
11AK52 BLOCK SCHEME

25.12.2002

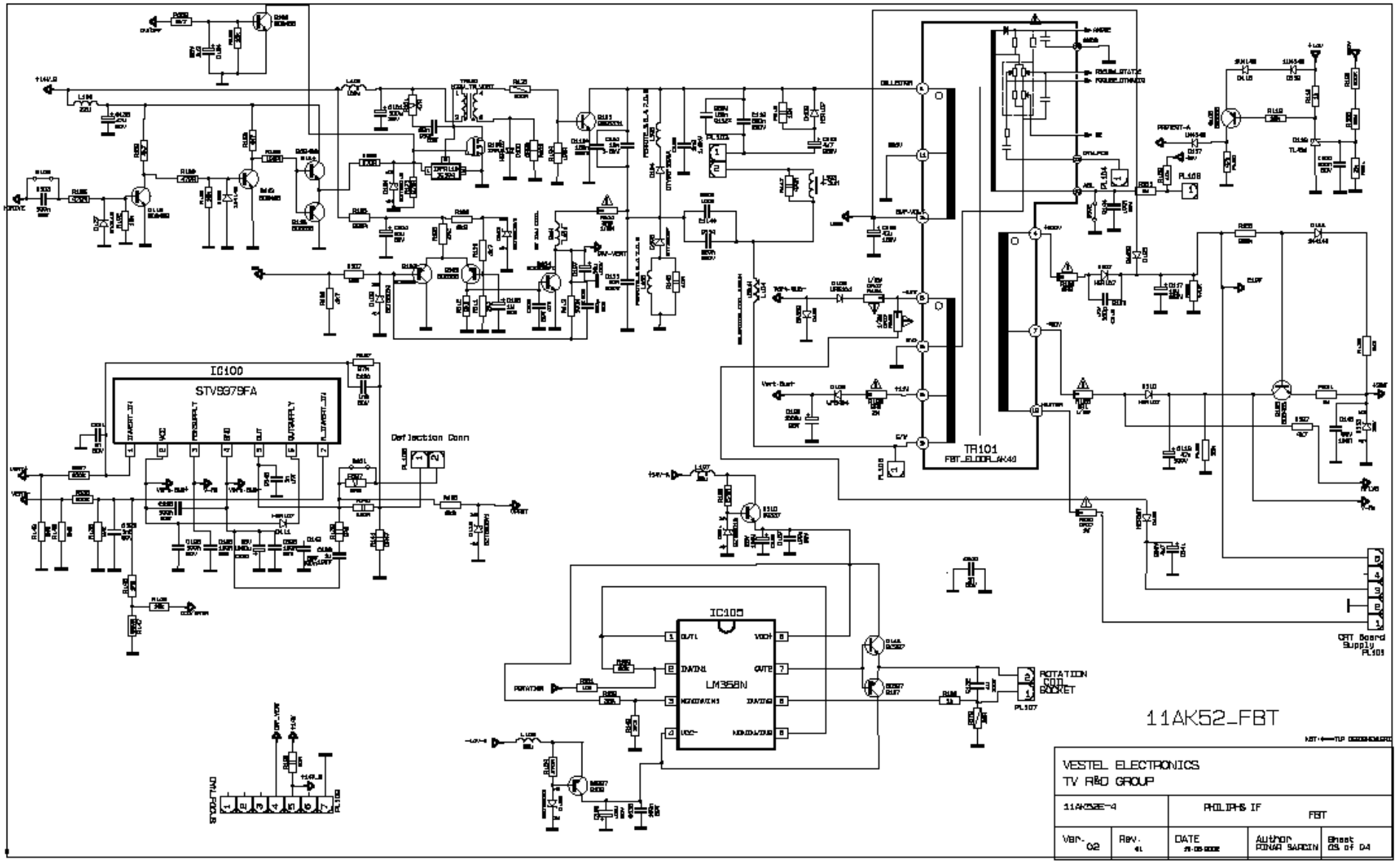
18.CIRCUIT DIAGRAMS



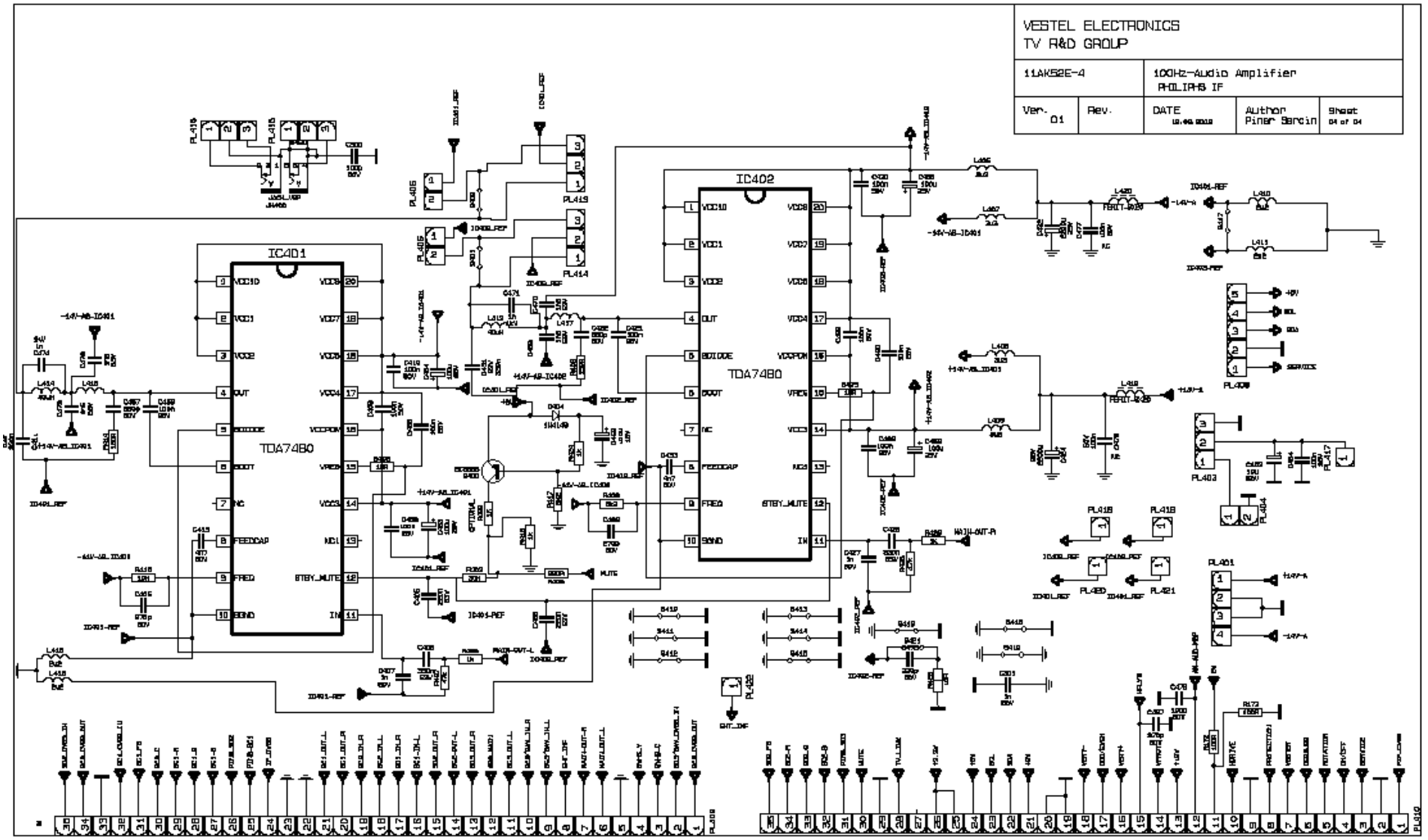
11ak52b4-VIDEO



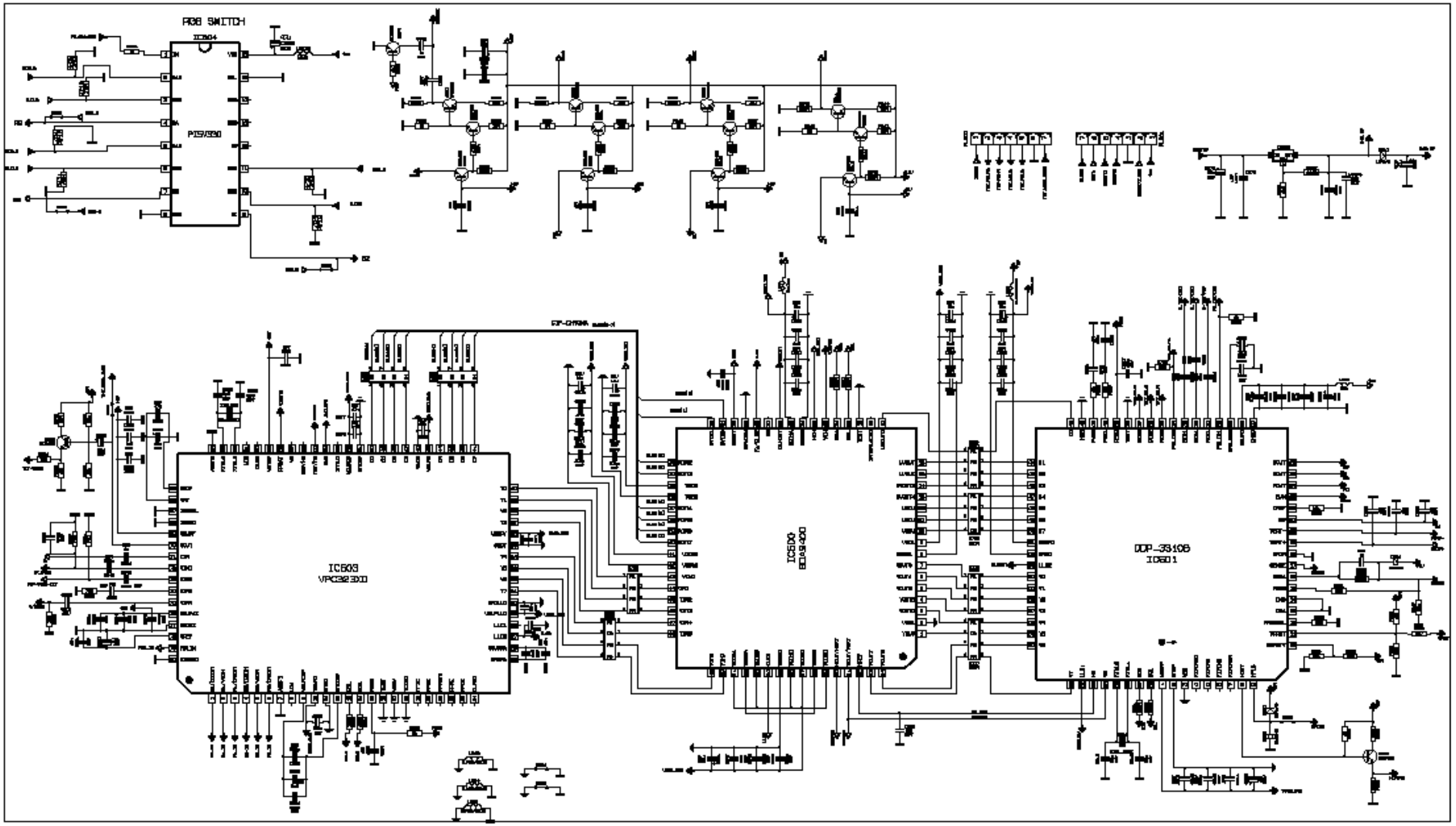
11ak52b4-2


IC100
STV9379FA
Deflection Conn
IC105
LM358N
TR101
FBT_ELDOR_AK40
ROTATION COIL SOCKET
CRT Board Supply
11AK52_FBT
VESTEL ELECTRONICS
TV R&D GROUP
PHILIPS IF
FBT

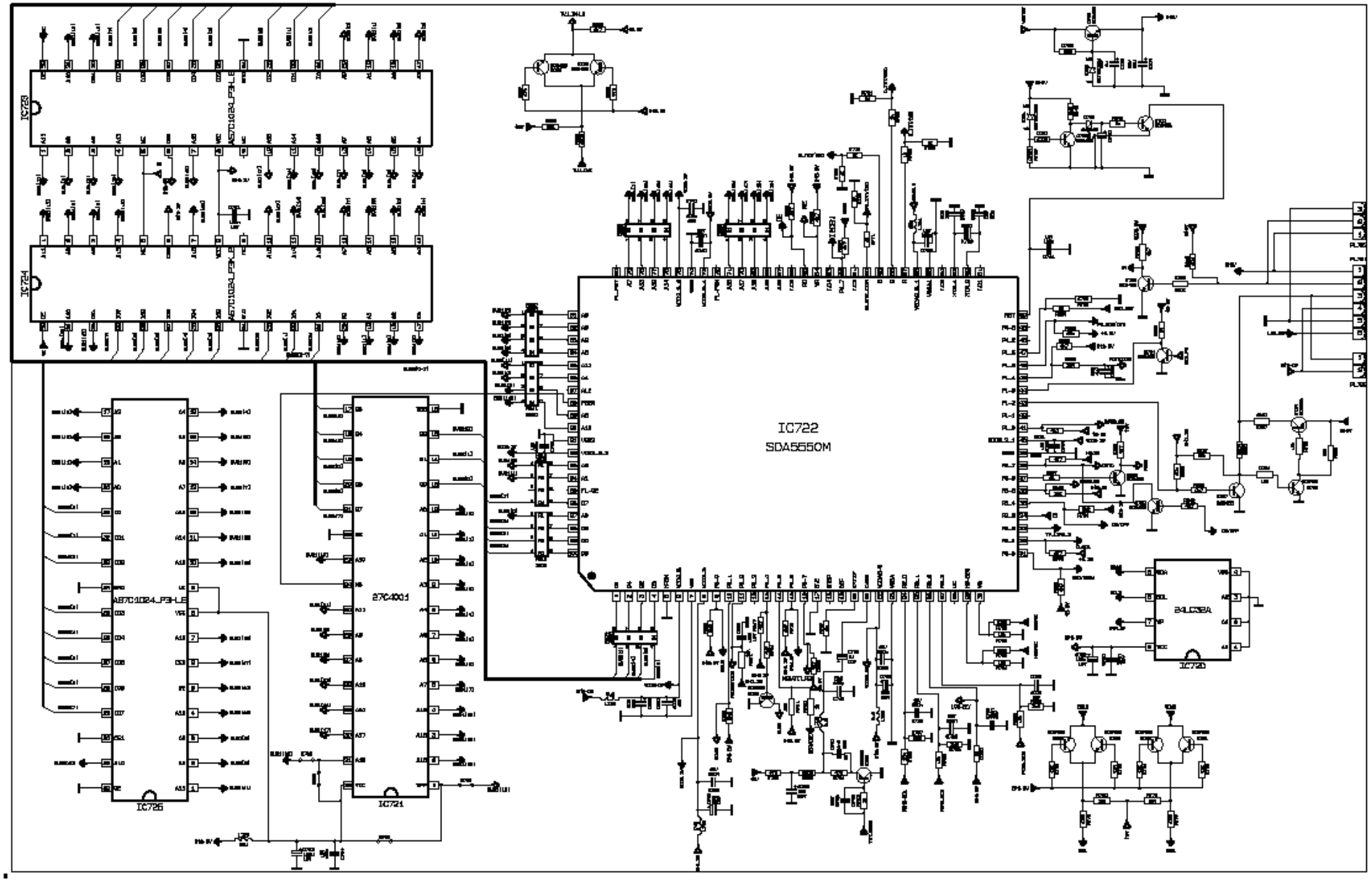
11ak52b4-3


VESTEL ELECTRONICS
TV R&D GROUP
11AK52E-4
100Hz-Audio Amplifier
PHILIPHS IF
Ver. 01
Rev.
DATE
Author
Piner Sercin
Sheet
04 of 04
IC401
TDA7480
IC402
TDA7480

11ak52b4-4



11fb2a3—1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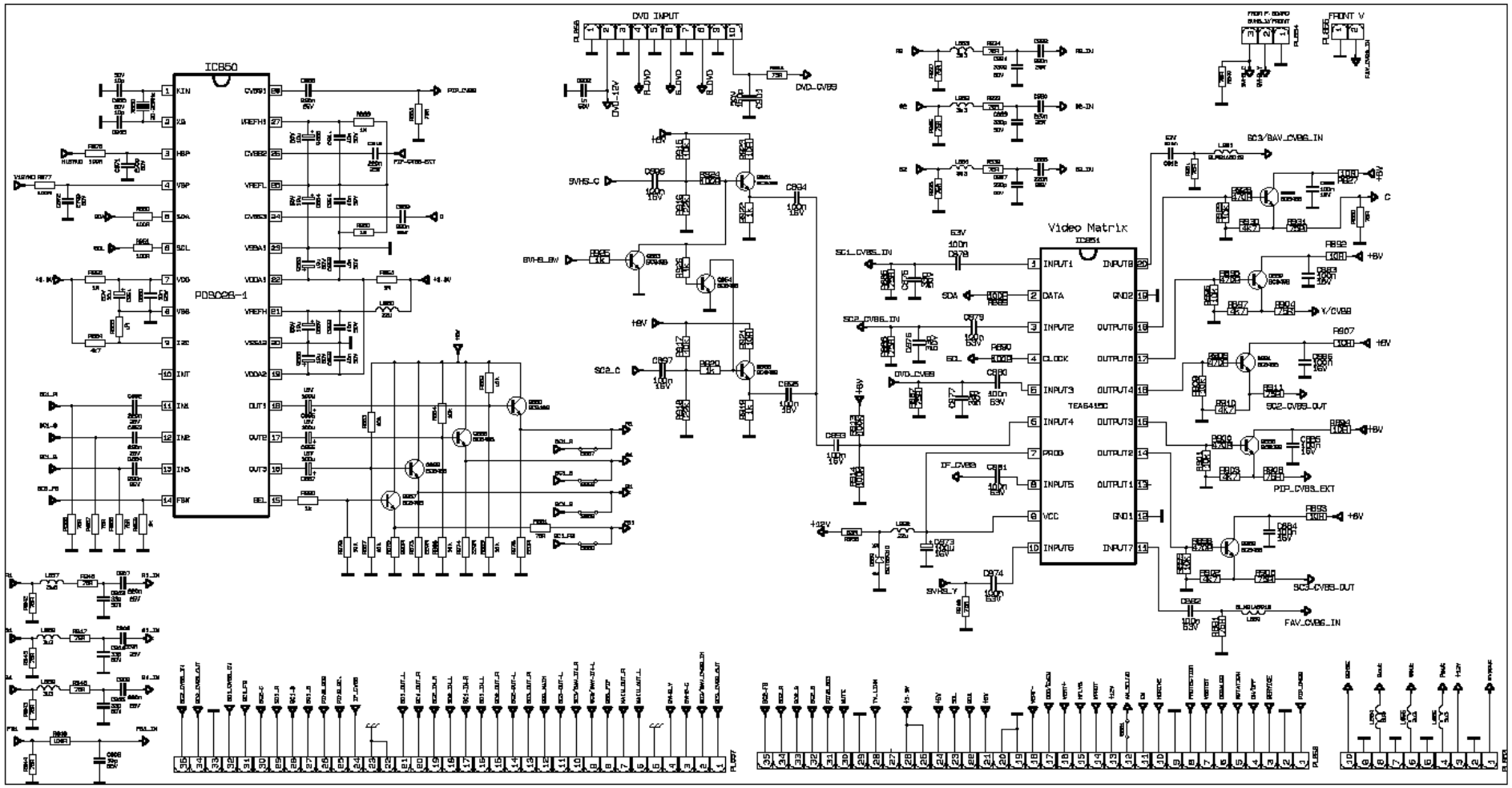
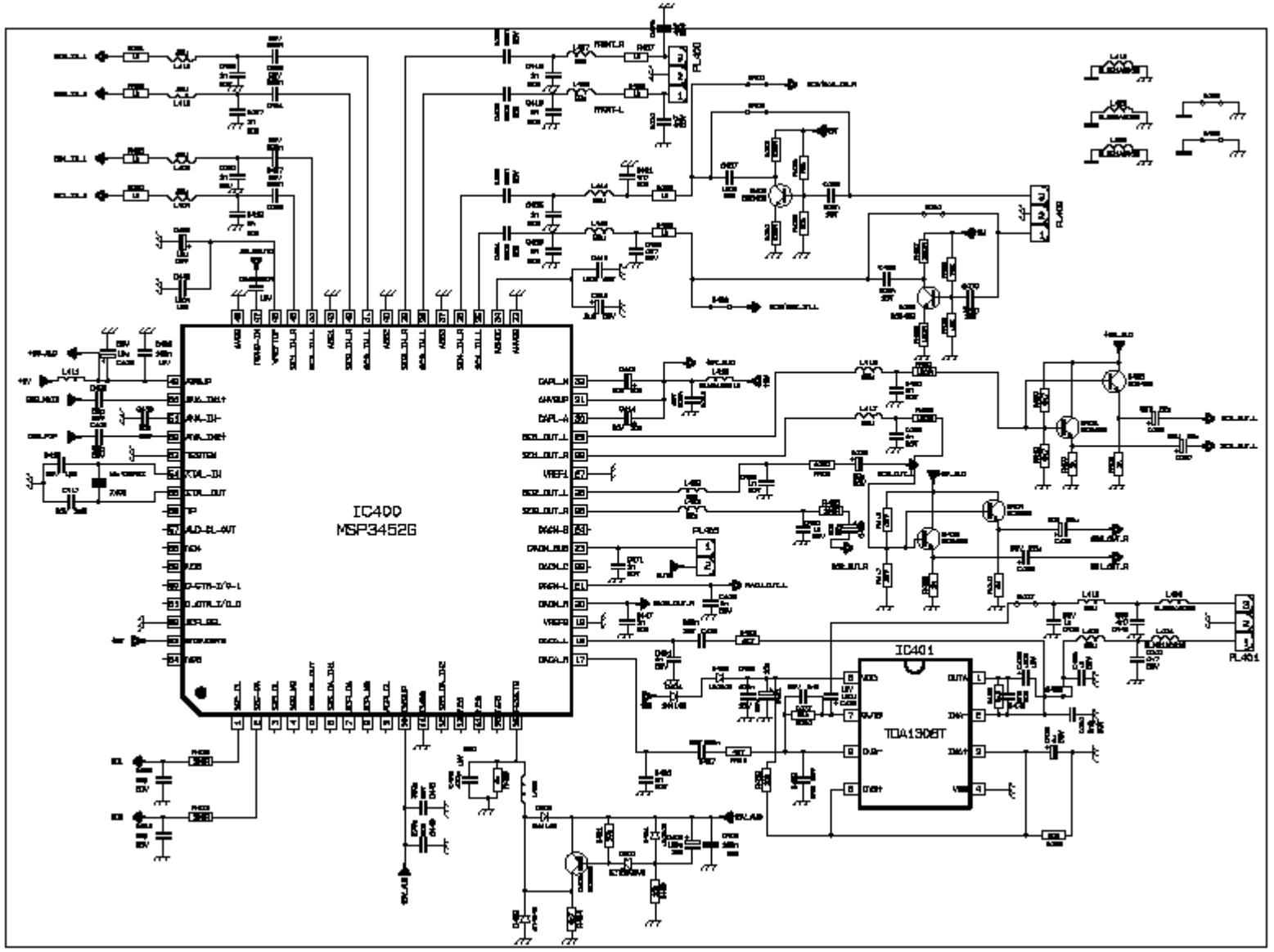
SDA5550M
IC725
IC724
IC721
IC720
A57D1024_F3H_LE
27C4001
24LC32A


DVD INPUT
ICB50
PDB0028-1
Video Matrix
TEA6415C
INPUT1
INPUT2
INPUT3
INPUT4
INPUT5
INPUT6
INPUT7
INPUT8
OUTPUT1
OUTPUT2
OUTPUT3
OUTPUT4
OUTPUT5
OUTPUT6
DATA
CLOCK
SDA
SCL
SC1_CVBS_IN
SC2_CVBS_IN
DVD_CVBS
SVHS-C
SVHS-Y
SC3/BAV_CVBS_IN
FAV_CVBS_IN
SC2_CVBS_OUT
SC3_CVBS_OUT
PIP_CVBS_EXT
Y/CVBS
C
+8V
+5V

11fb2a3—3



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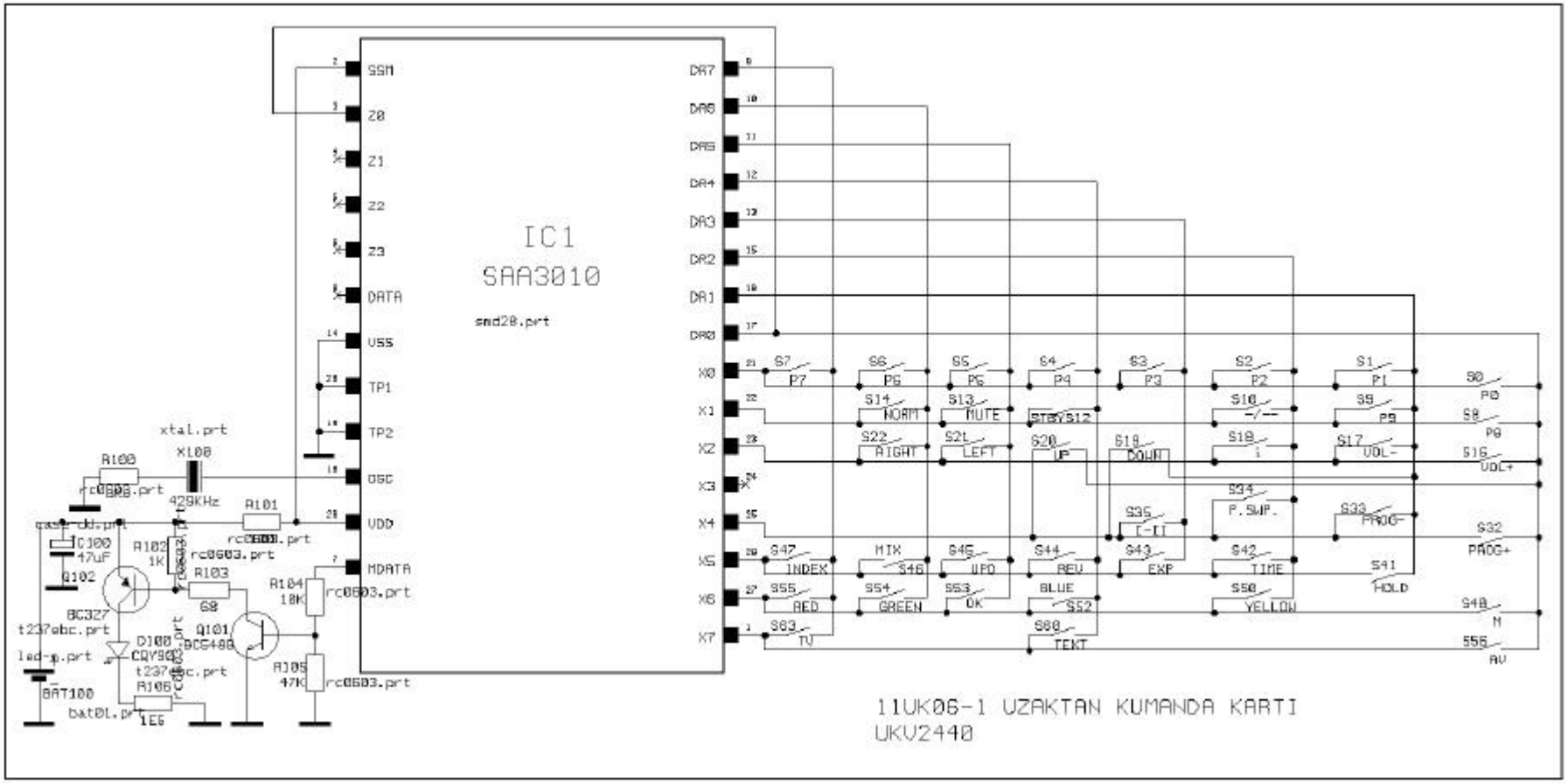
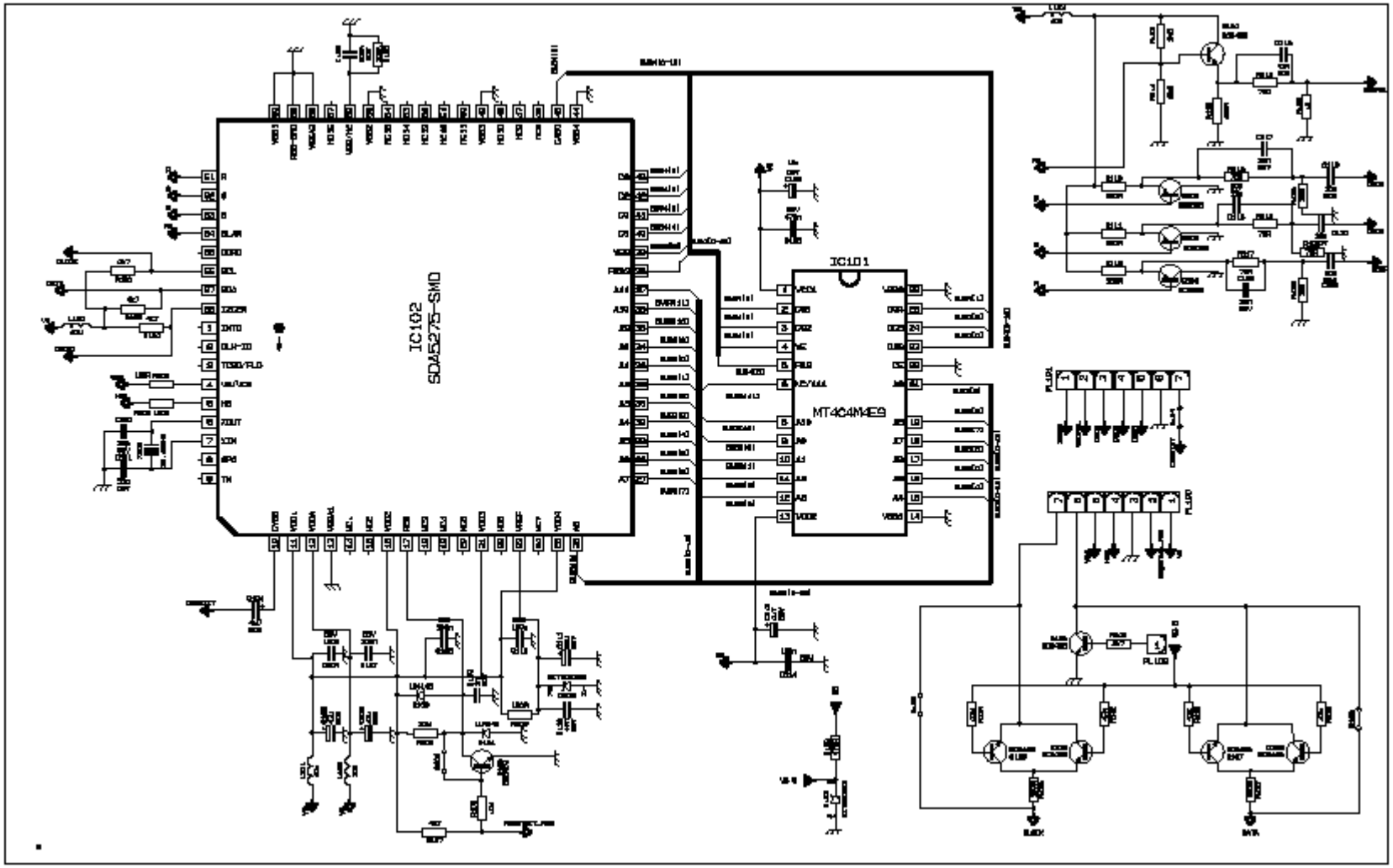
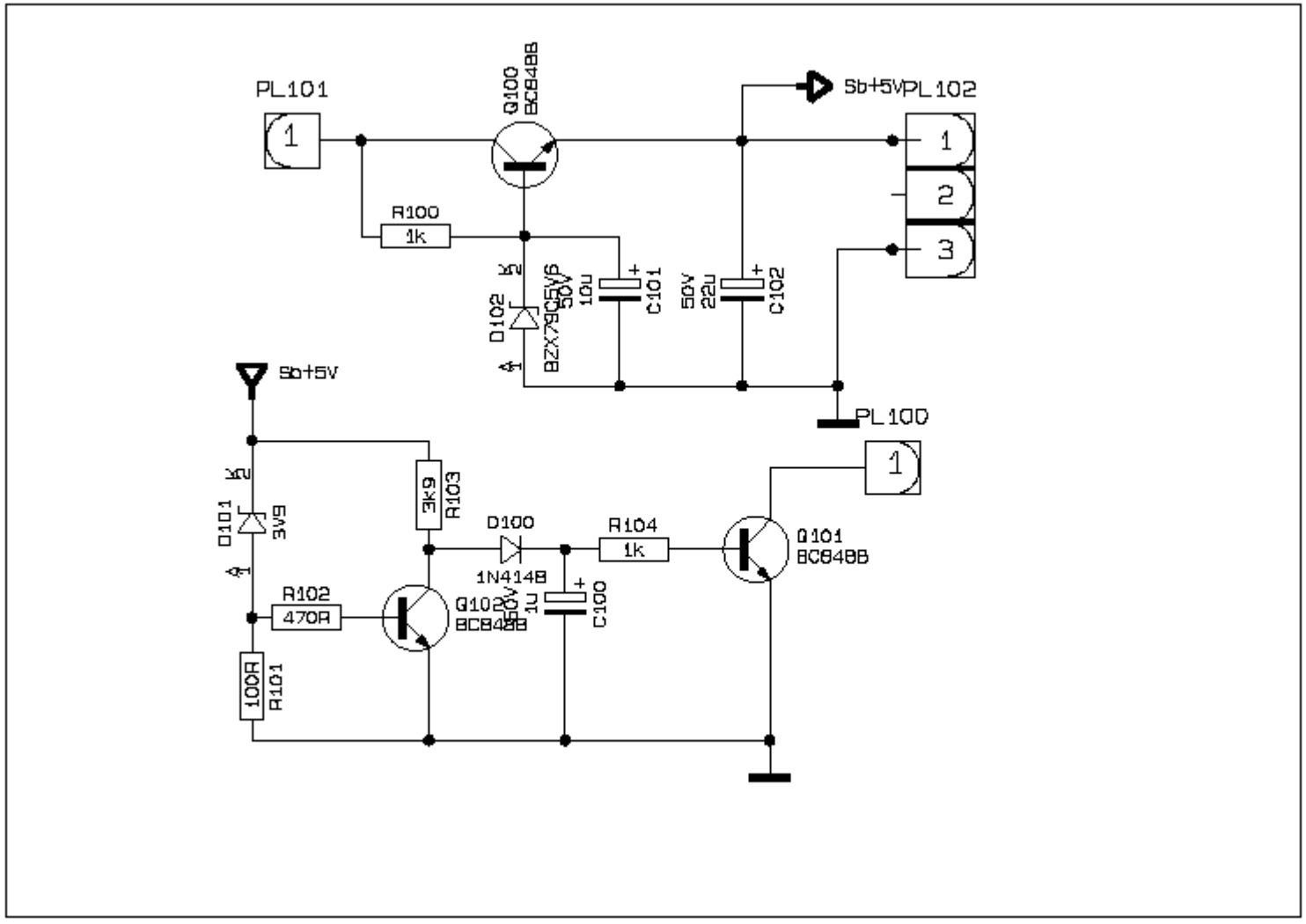

IC1
SAA3010
smd28.prt
SSM
Z0
Z1
Z2
Z3
DATA
VSS
TP1
TP2
OSC
VDD
MDATA
DR7
DR6
DR5
DR4
DR3
DR2
DR1
DR0
X0
X1
X2
X3
X4
X5
X6
X7
xtal.prt
X100
429KHz
R100
R101
R102
1K
R103
68
R104
18K
R105
47K
C100
47uF
Q102
BC327
Q101
BC548
D100
CRY903
BAT100
bat0l.prt
led-g.prt
S7 P7
S6 P6
S5 P5
S4 P4
S3 P3
S2 P2
S1 P1
S0 P0
S14 NORM
S13 MUTE
S12
S10 -/--
S9 P9
S8 P8
S22 RIGHT
S21 LEFT
S20 UP
S19 DOWN
S18 i
S17 VOL-
S16 VOL+
S34 P.SWP.
S35 [-I]
S33 PROG-
S32 PROG+
S47 INDEX
S46 MIX
S45 UPD
S44 REV
S43 EXP
S42 TIME
S41 HOLD
S55 RED
S54 GREEN
S53 OK
S52 BLUE
S50 YELLOW
S49 M
S48
S83 TV
S80 TEXT
555 AV
11UK06-1 UZAKTAN KUMANDA KARTI
UKU2440

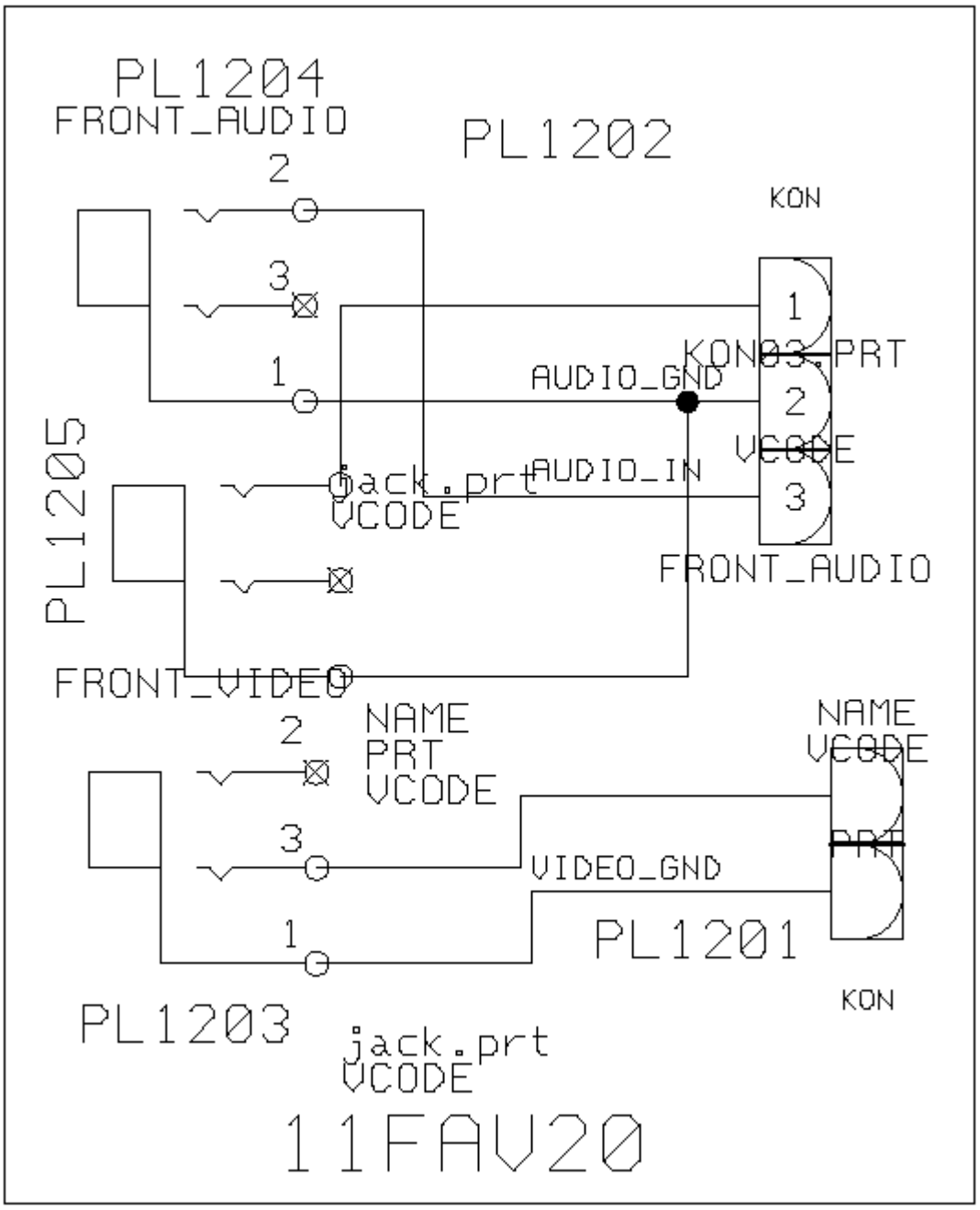
11uk06-1



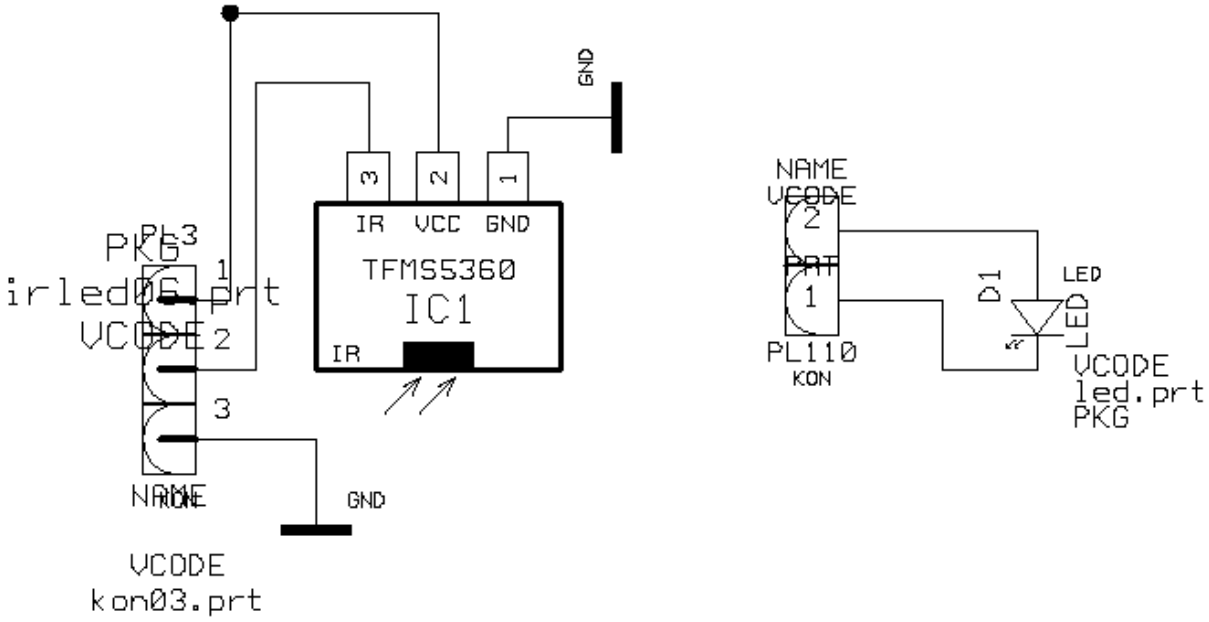
11txt52-4


PL101
1
Q100
BC848B
Sb+5V
PL102
1
2
3
R100
1k
D102
BZX79C5V6
5V6
C101
10u
50V
C102
22u
50V
PL100
Sb+5V
D101
3V9
R103
3K9
D100
1N4148
R104
1k
Q101
BC848B
1
R102
470R
Q102
BC848B
C100
1u
50V
R101
100R

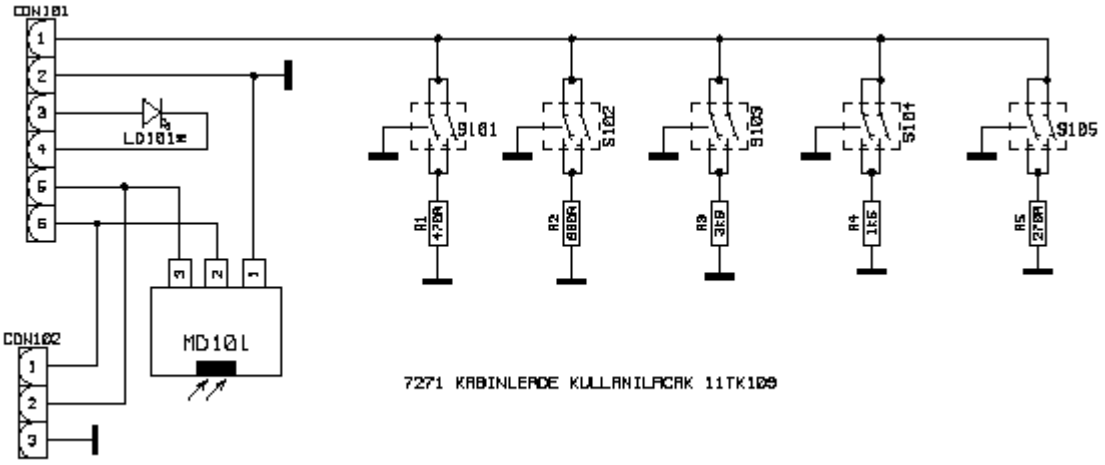
11rs52


PL1204
FRONT_AUDIO
PL1202
KON
2
3
1
1
KON03.PRT
AUDIO_GND
2
VCODE
AUDIO_IN
3
jack.prt
VCODE
PL1205
FRONT_AUDIO
FRONT_VIDEO
2
NAME
PRT
VCODE
NAME
VCODE
3
VIDEO_GND
PRT
1
PL1201
KON
PL1203
jack.prt
VCODE
11FAV20

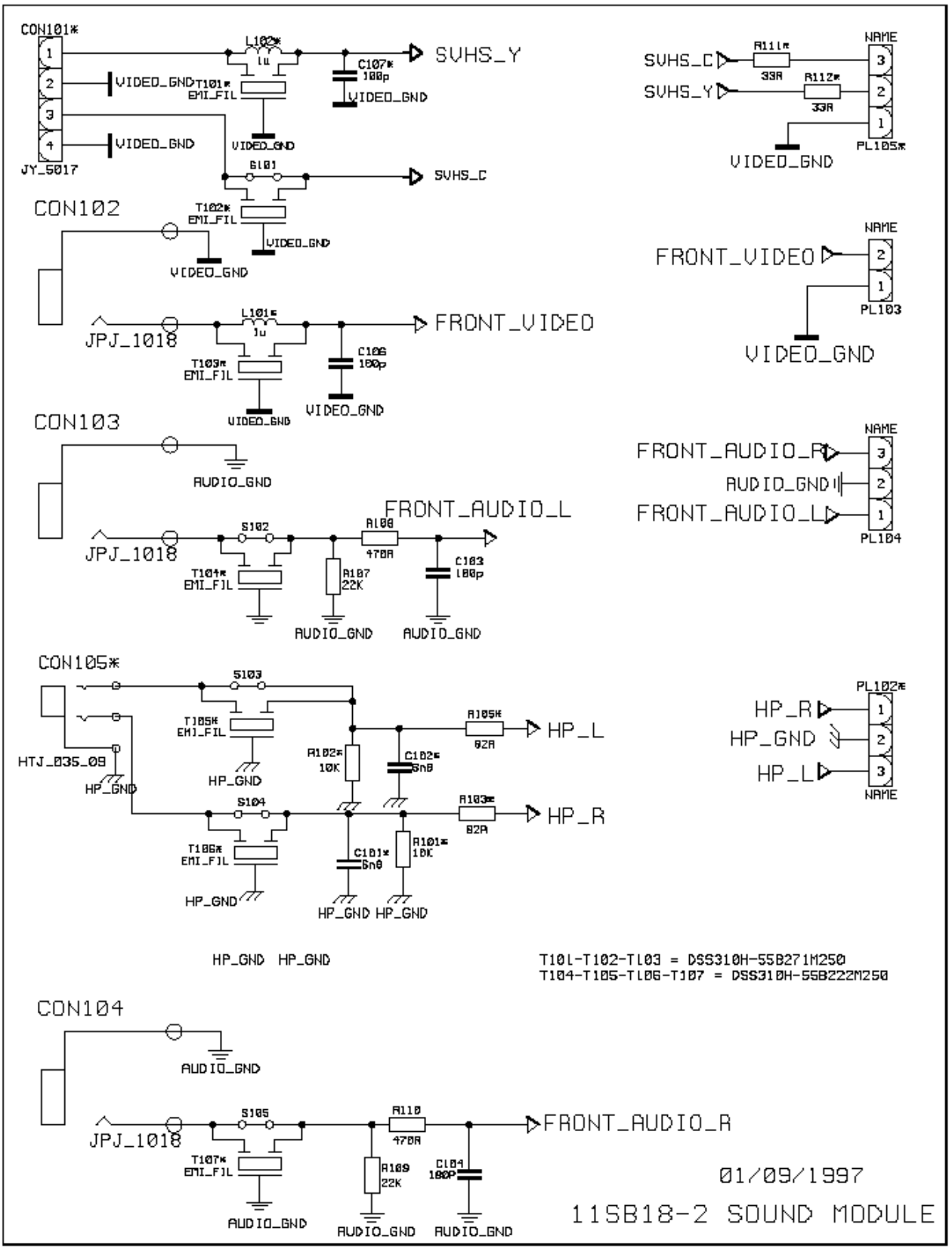
11fav19a4



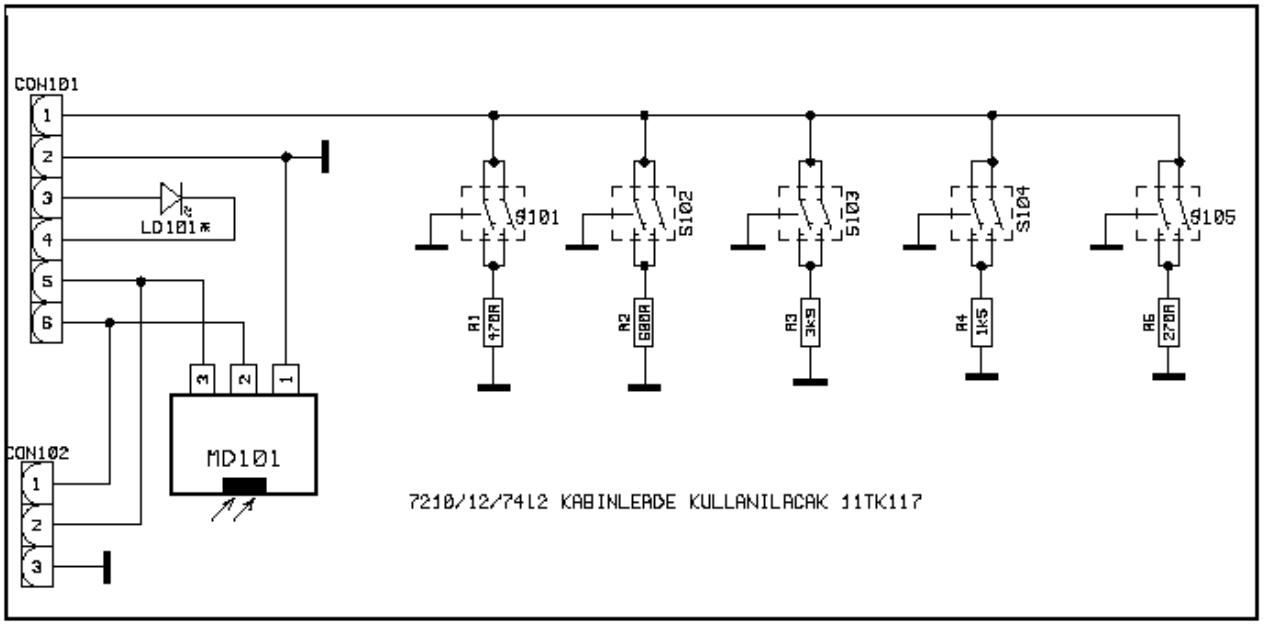
11ir2872



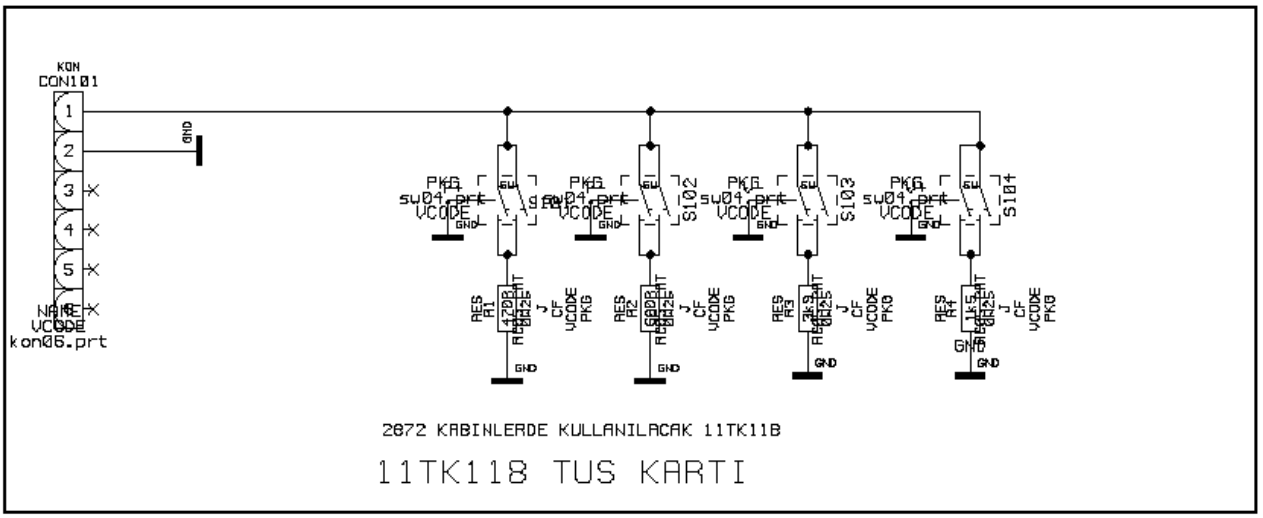
11tk109


CON101*
JY_5017
L102*
1u
C107*
100p
SVHS_Y
VIDEO_GND
T101*
EMI_FIL
VIDEO_GND
VIDEO_GND
G101
SVHS_C
CON102
T102*
EMI_FIL
VIDEO_GND
VIDEO_GND
JPJ_1018
L101*
1u
FRONT_VIDEO
T103*
EMI_FIL
C106
100p
VIDEO_GND
VIDEO_GND
CON103
AUDIO_GND
FRONT_AUDIO_L
JPJ_1018
S102
R108
470R
T104*
EMI_FIL
R107
22K
C103
100p
AUDIO_GND
AUDIO_GND
CON105*
S103
T105*
EMI_FIL
R105*
82R
HP_L
HTJ_035_09
HP_GND
R102*
10K
C102*
5n6
S104
R103*
82R
HP_R
T106*
EMI_FIL
C101*
5n6
R101*
10K
HP_GND
HP_GND
HP_GND
HP_GND HP_GND
T101-T102-T103 = DSS310H-55B271M250
T104-T105-T106-T107 = DSS310H-55B222M250
CON104
AUDIO_GND
JPJ_1018
S105
R110
470R
FRONT_AUDIO_R
T107*
EMI_FIL
R109
22K
C104
100P
AUDIO_GND
AUDIO_GND
AUDIO_GND
01/09/1997
11SB18-2 SOUND MODULE
SVHS_C
SVHS_Y
R111*
33R
R112*
33R
NAME
PL105*
VIDEO_GND
FRONT_VIDEO
NAME
PL103
VIDEO_GND
FRONT_AUDIO_R
AUDIO_GND
FRONT_AUDIO_L
NAME
PL104
PL102*
HP_R
HP_GND
HP_L
NAME

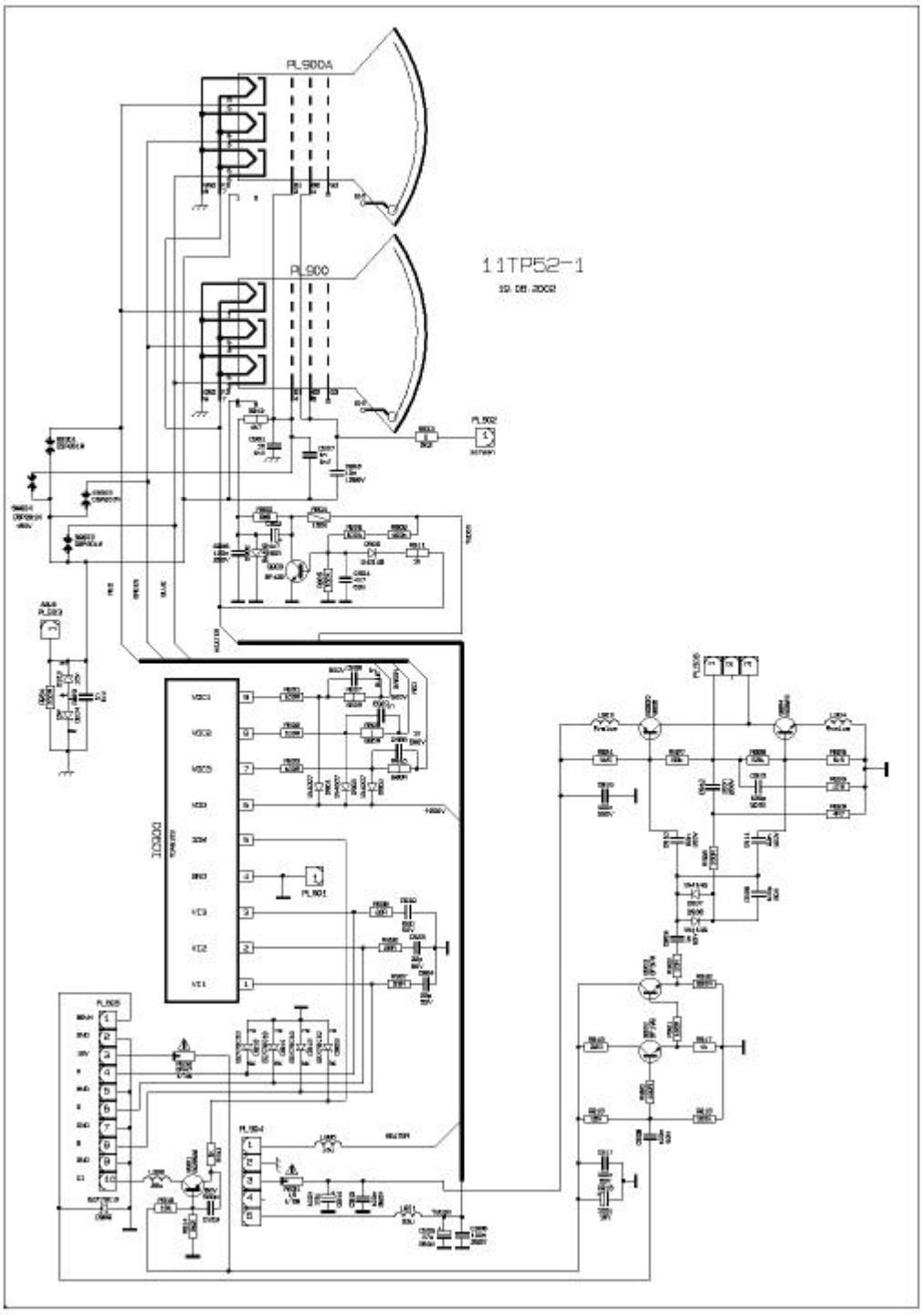
11sb18-3



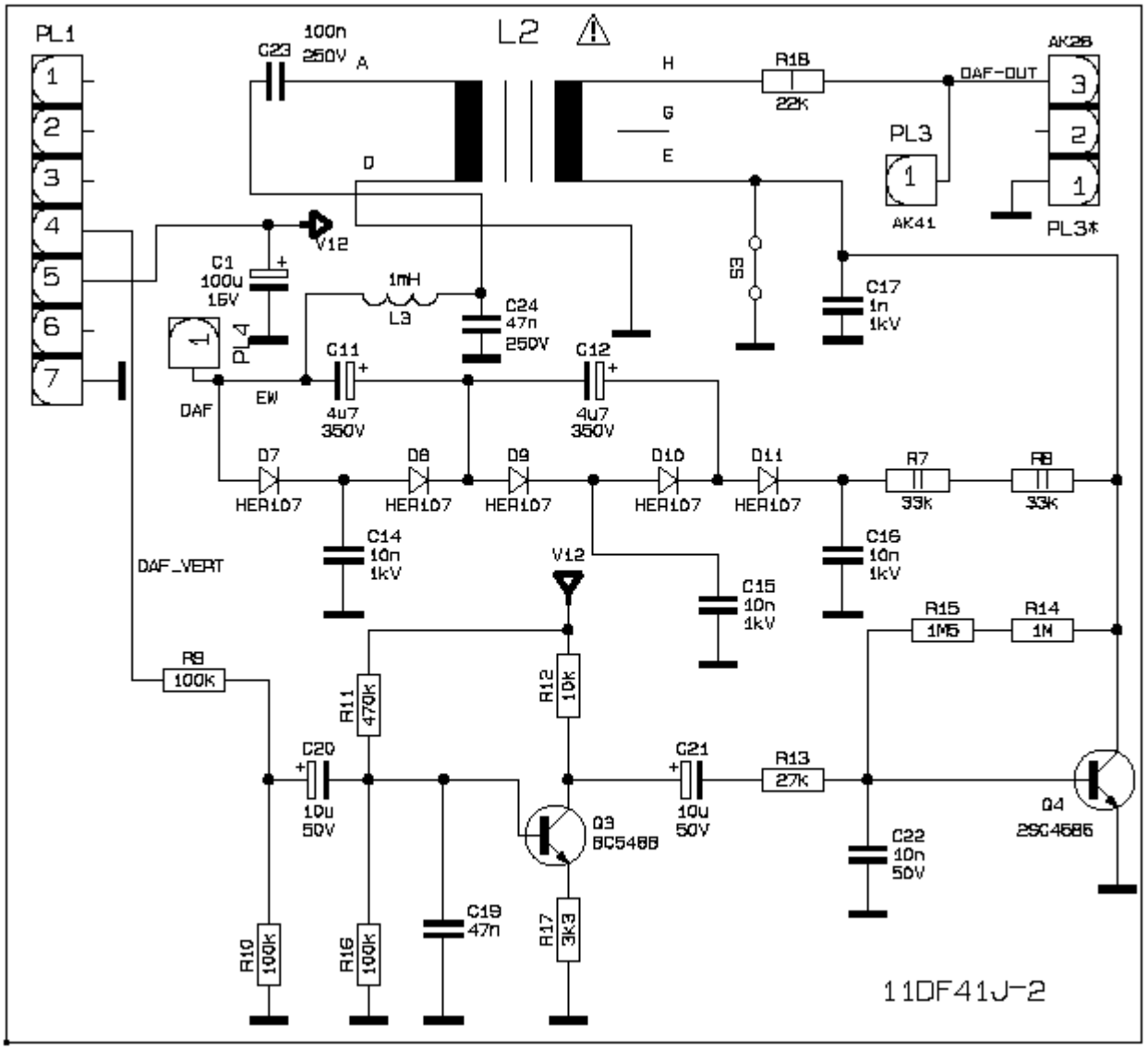
11tk117



11tk118



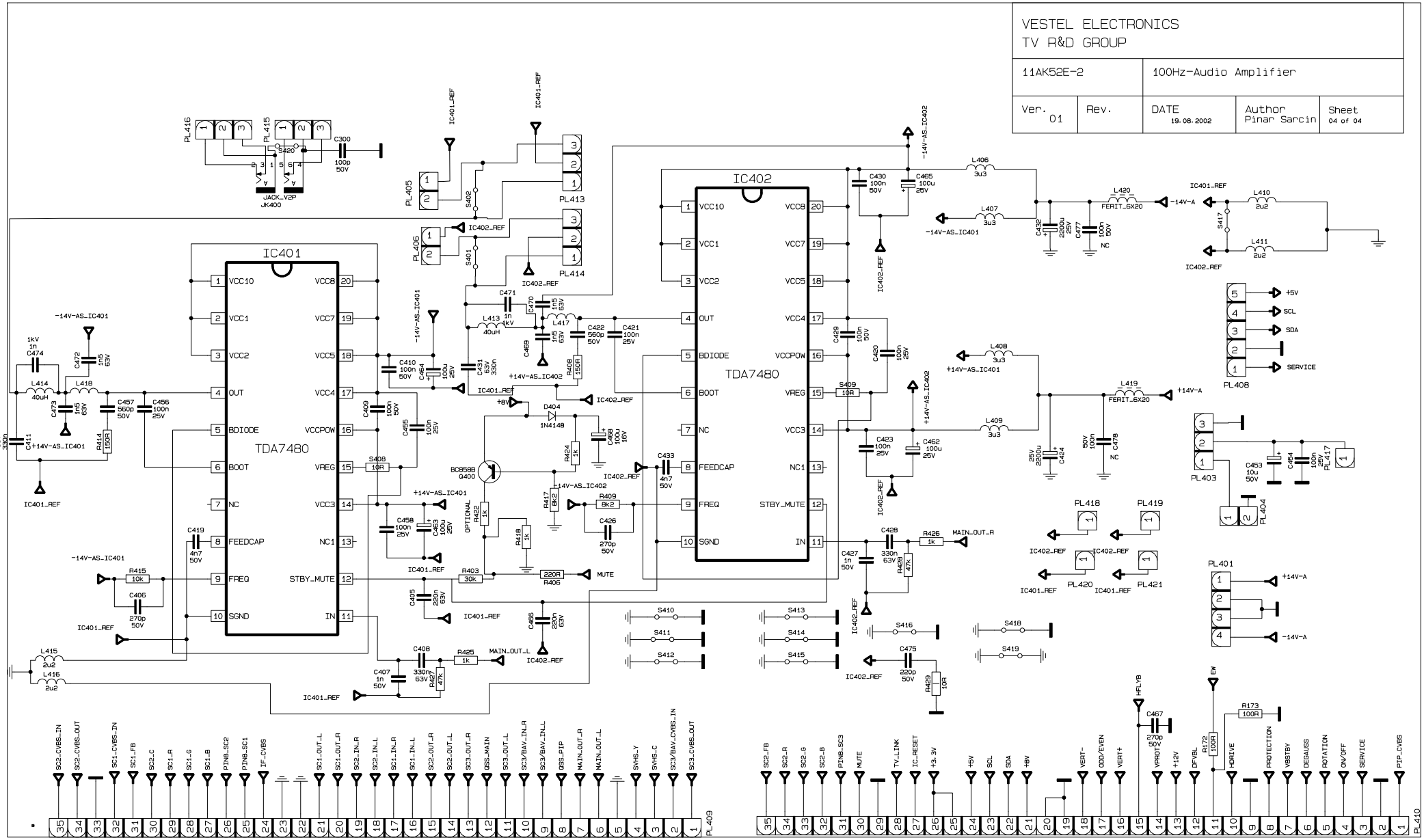
11tp52-1

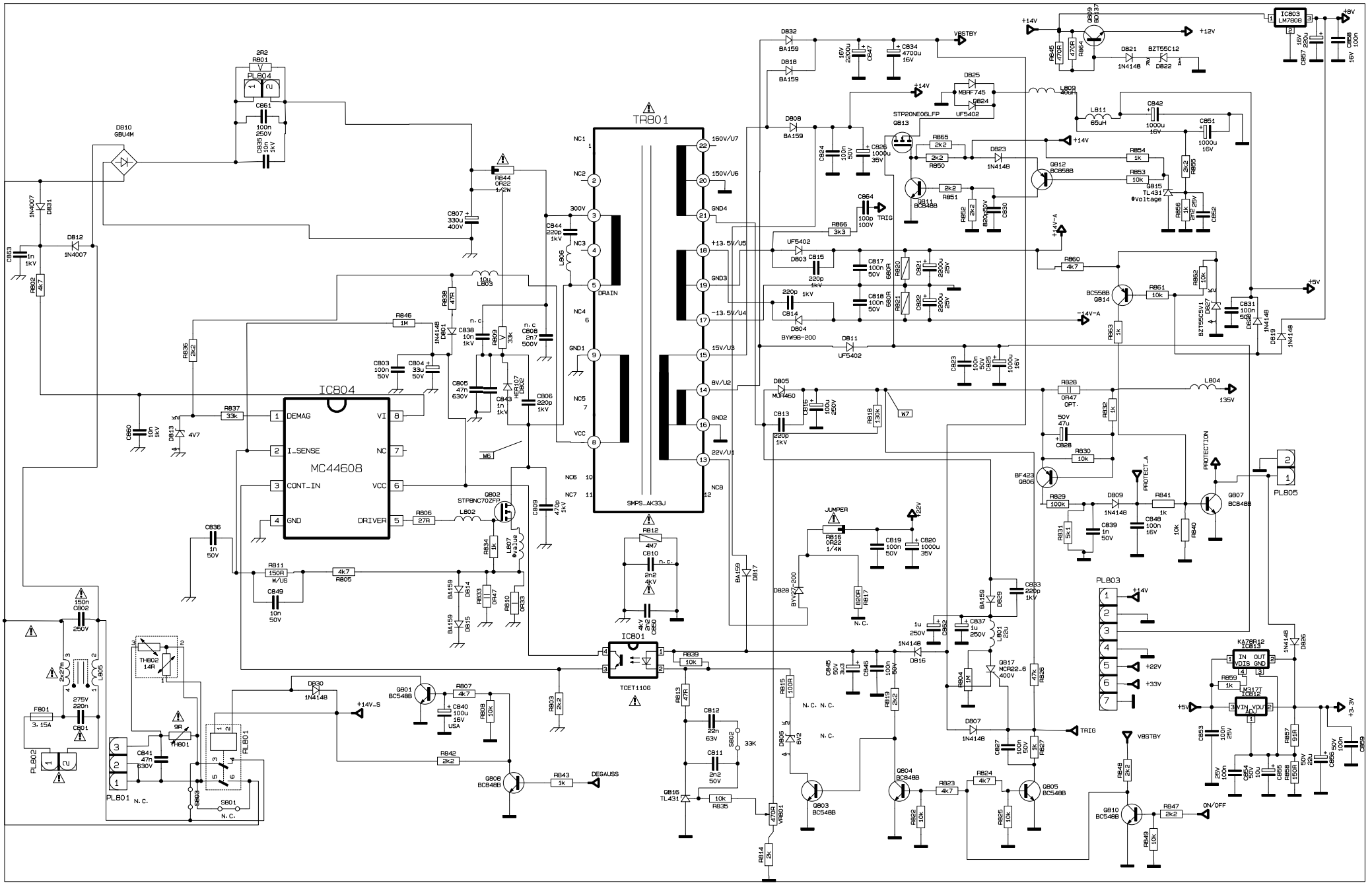

PL1
C23 100n 250V
L2
A
H
R18 22K
DAF-OUT
AK26
PL3
AK41
PL3*
G
E
D
V12
C1 100u 16V
1mH
L3
C24 47n 250V
PL4
C11 4u7 350V
C12 4u7 350V
S3
C17 1n 1kV
DAF
EW
D7 HER107
D8 HER107
D9 HER107
D10 HER107
D11 HER107
R7 33K
R8 33K
C14 10n 1kV
C16 10n 1kV
C15 10n 1kV
DAF_VERT
R15 1M5
R14 1M
R9 100K
R11 470K
R12 10K
C20 10u 50V
C21 10u 50V
R13 27K
Q3 BC548B
Q4 2SC4686
C22 10n 50V
C19 47n
R17 3K3
R10 100K
R16 100K
11DF41J-2

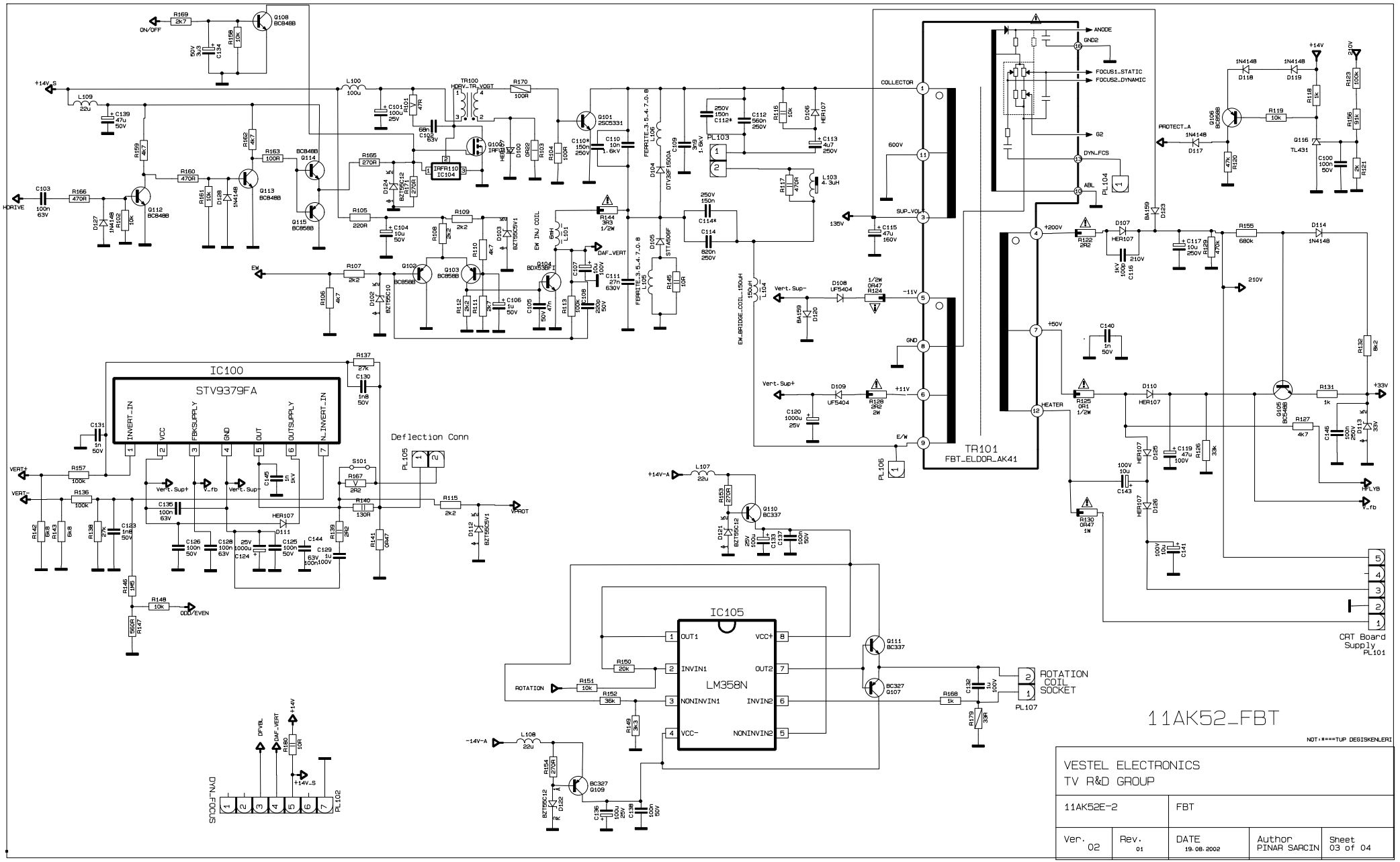
11df41j-2

Schematics

AK52-1


VESTEL ELECTRONICS
TV R&D GROUP
11AK52E-2
100Hz-Audio Amplifier
Ver. 01
Rev.
DATE 19.08.2002
Author Pinar Sarcin
Sheet 04 of 04
IC401
IC402
TDA7480
VCC10
VCC1
VCC2
OUT
BDIODE
BOOT
NC
FEEDCAP
FREQ
SGND
VCC8
VCC7
VCC5
VCC4
VCCPOW
VREG
VCC3
NC1
STBY_MUTE
IN
-14V-AS_IC401
-14V-AS_IC402
+14V-AS_IC401
+14V-AS_IC402
IC401_REF
IC402_REF
+8V
+5V
SCL
SDA
SERVICE
+14V-A
MUTE
MAIN_OUT_L
MAIN_OUT_R
PL401
PL403
PL404
PL405
PL406
PL408
PL409
PL410
PL413
PL414
PL415
PL416
PL417
PL418
PL419
PL420
PL421
JK400
S401
S402
S408
S409
S410
S411
S412
S413
S414
S415
S416
S418
S419
S420
D404
1N4148
BC858B
Q400
OPTIONAL
SC2_CVBS_IN
SC2_CVBS_OUT
SC1_CVBS_IN
SC1_FB
SC2_C
SC1_R
SC1_G
SC1_B
PIN8_SC2
PIN8_SC1
IF_CVBS
SC1_OUT_L
SC1_OUT_R
SC2_IN_R
SC2_IN_L
SC1_IN_R
SC1_IN_L
SC2_OUT_R
SC2_OUT_L
SC3_OUT_R
QSS_MAIN
SC3_OUT_L
SC3/BAV_IN_R
SC3/BAV_IN_L
QSS_PIP
MAIN_OUT_R
MAIN_OUT_L
SVHS_Y
SVHS_C
SC3/BAV_CVBS_IN
SC3_CVBS_OUT
SC2_FB
SC2_R
SC2_G
SC2_B
PIN8_SC3
MUTE
TV_LINK
IC_RESET
+3.3V
+5V
SCL
SDA
+8V
VERT-
ODD/EVEN
VERT+
VPROT
+12V
DFVBL
HFLYB
EW
HDRIVE
PROTECTION
VBSTBY
DEGAUSS
ROTATION
ON/OFF
SERVICE
PIP_CVBS


IC804
MC44608
DEMAG
I_SENSE
CONT_IN
GND
VI
NC
VCC
DRIVER
TR801
SMPS_4K33J
DRAIN
160V/U7
150V/U6
+13.5V/U5
-13.5V/U4
15V/U3
8V/U2
22V/U1
IC801
TCET110G
Q802
STP8NC70ZFP
Q813
STP20NE06LFP
IC803
LM7808
PL804
PL805
PL803
PL801
PL802
JUMPER
W6
W7
DEGAUSS
TRIG
VBSTBY
ON/OFF
PROTECTION
PROTECT_A
+14V
+12V
+8V
+5V
+3.3V
+22V
+33V
135V
-14V-A
+14V-A
+14V-S
Voltage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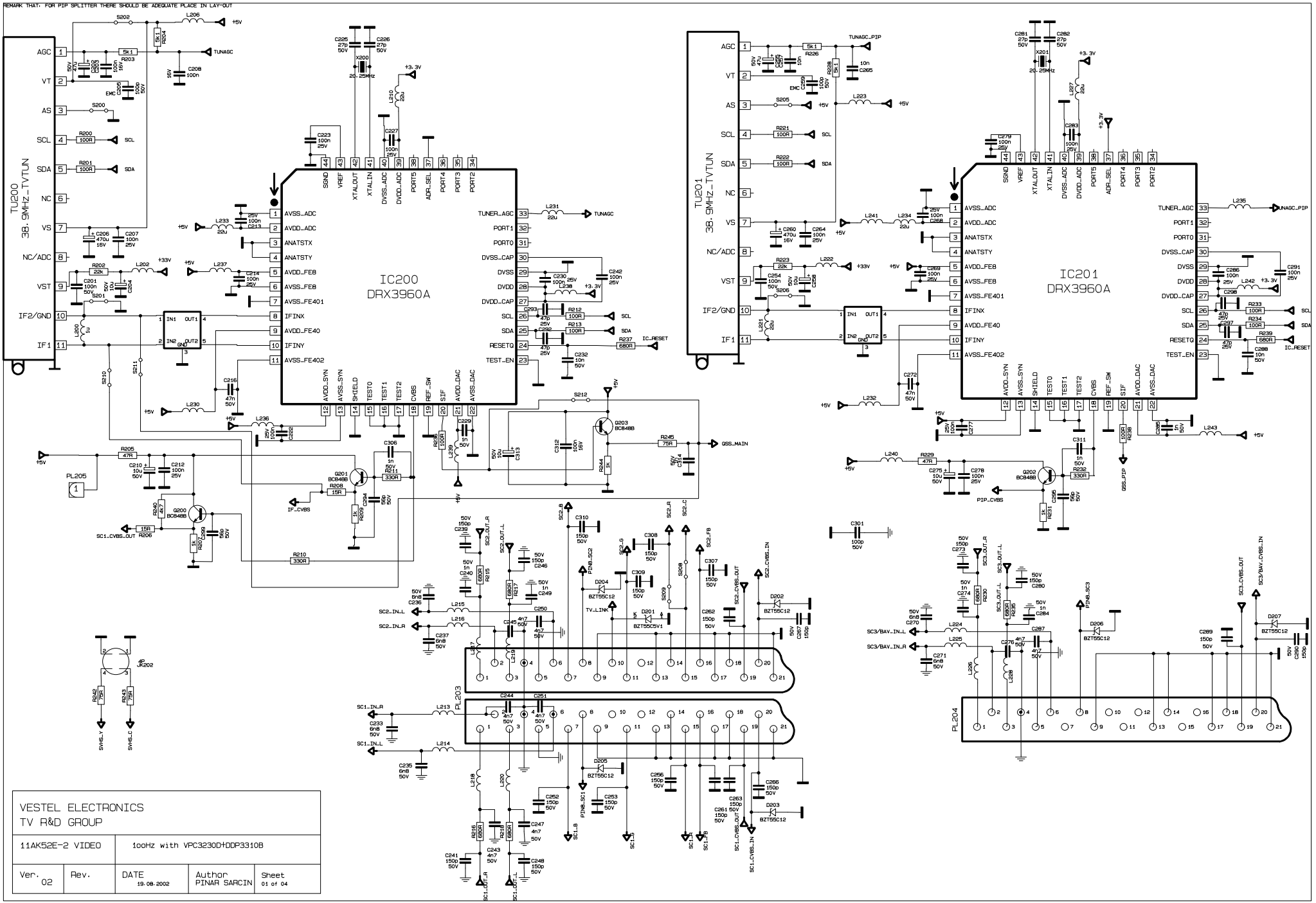
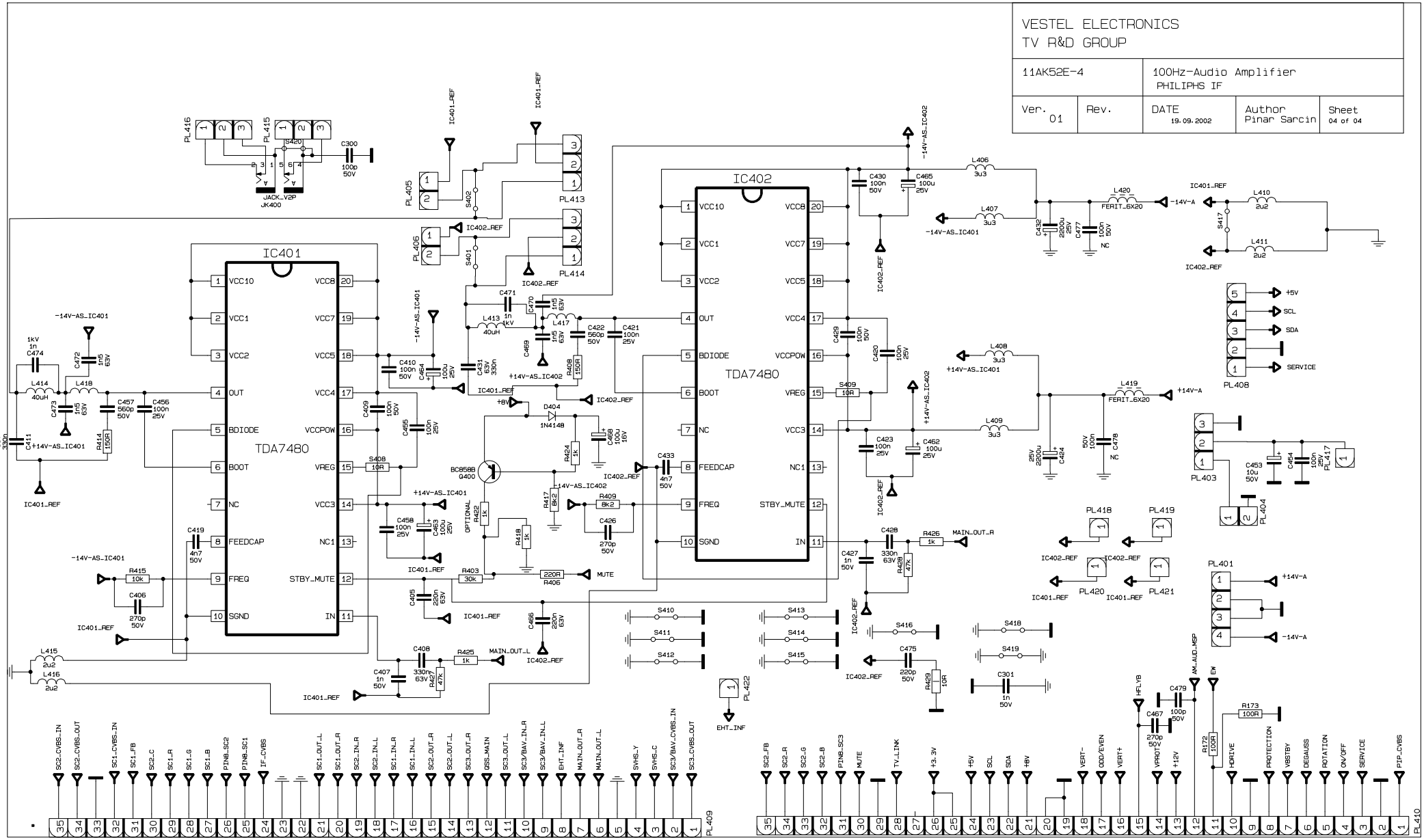
INVERT_IN
VCC
FBKSUPPLY
GND
OUT
OUTSUPPLY
N_INVERT_IN
Deflection Conn
IC105
LM358N
OUT1
INVIN1
NONINVIN1
VCC-
VCC+
OUT2
INVIN2
NONINVIN2
TR101
FBT_ELDOR_AK41
COLLECTOR
600V
SUP_VOL
135V
GND
E/W
HEATER
ANODE
GND2
FOCUS1_STATIC
FOCUS2_DYNAMIC
G2
DYN_FCS
ABL
+200V
+50V
+11V
-11V
+33V
210V
PROTECT_A
HFLYB
V_fb
ROTATION COIL SOCKET
PL107
CRT Board Supply
PL101
DYN_FOCUS
PL102
ON/OFF
+14V_S
HDRIVE
EW
DAF_VERT
VERT+
VERT-
ODD/EVEN
VFROT
-14V-A
+14V-A
ROTATION
11AK52_FBT
NOT:*===TUP DEGISKENLERI
VESTEL ELECTRONICS
TV R&D GROUP
11AK52E-2
FBT
Ver. 02
Rev. 01
DATE 19.08.2002
Author PINAR SARCIN
Sheet 03 of 04

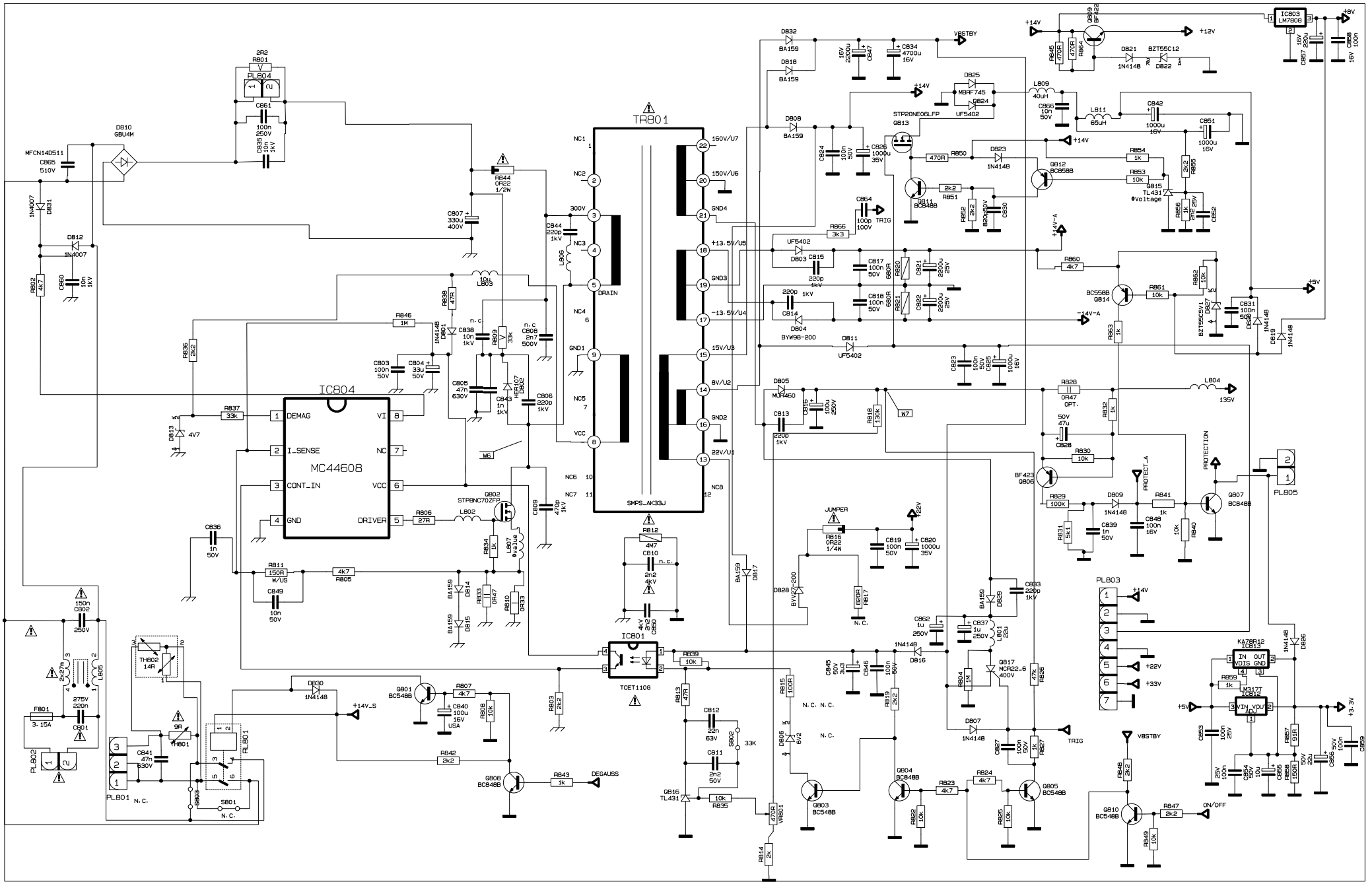
REMARK THAT, FOR PIP SPLITTER THERE SHOULD BE ADEQUATE PLACE IN LAY-OUT



VESTEL ELECTRONICS TV R&D GROUP				
11AK52E-2 VIDEO		100Hz with VPC3230D+DDP3310B		
Ver. 02	Rev.	DATE 19.08.2002	Author PINAR SARCIN	Sheet 01 of 04

AK52-B2


VESTEL ELECTRONICS
TV R&D GROUP
11AK52E-4
100Hz-Audio Amplifier
PHILIPHS IF
Ver. 01
Rev.
DATE 19.09.2002
Author Pinar Sarcin
Sheet 04 of 04
IC401
IC402
TDA7480
VCC10
VCC1
VCC2
OUT
BDIODE
BOOT
NC
FEEDCAP
FREQ
SGND
VCC8
VCC7
VCC5
VCC4
VCCPOW
VREG
VCC3
NC1
STBY_MUTE
IN
-14V-AS_IC401
-14V-AS_IC402
+14V-AS_IC401
+14V-AS_IC402
IC401_REF
IC402_REF
+8V
MUTE
MAIN_OUT_L
MAIN_OUT_R
BC858B Q400
D404 1N4148
OPTIONAL
JACK_V2P JK400
PL405
PL406
PL413
PL414
PL415
PL416
PL408
PL403
PL404
PL417
PL418
PL419
PL420
PL421
PL401
PL422
PL409
PL410
EHT_INF
+5V
SCL
SDA
SERVICE
+14V-A
-14V-A
SC2_CVBS_IN
SC2_CVBS_OUT
SC1_CVBS_IN
SC1_FB
SC2_C
SC1_R
SC1_G
SC1_B
PIN8_SC2
PIN8_SC1
IF_CVBS
SC1_OUT_L
SC1_OUT_R
SC2_IN_R
SC2_IN_L
SC1_IN_R
SC1_IN_L
SC2_OUT_R
SC2_OUT_L
SC3_OUT_R
QSS_MAIN
SC3_OUT_L
SC3/BAV_IN_R
SC3/BAV_IN_L
EHT_INF
MAIN_OUT_R
MAIN_OUT_L
SVHS_Y
SVHS_C
SC3/BAV_CVBS_IN
SC3_CVBS_OUT
SC2_FB
SC2_R
SC2_G
SC2_B
PIN8_SC3
MUTE
TV_LINK
+3.3V
+5V
SCL
SDA
+8V
VERT-
ODD/EVEN
VERT+
VPROT
+12V
AM_AUD_MSP
EW
HFLYB
HDRIVE
PROTECTION
VBSTBY
DEGAUSS
ROTATION
ON/OFF
SERVICE
PIP_CVBS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DEMAG
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CONT_IN
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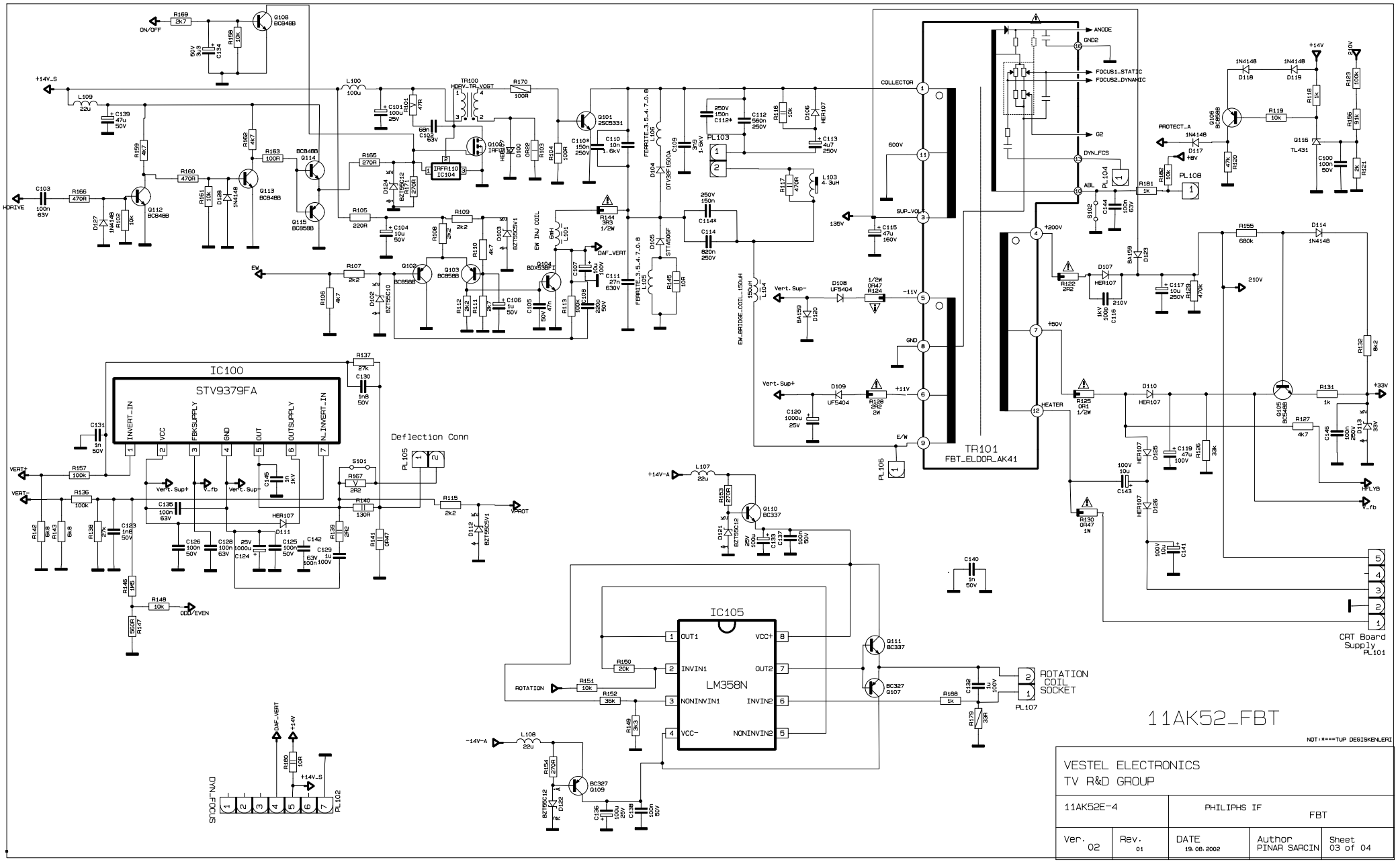
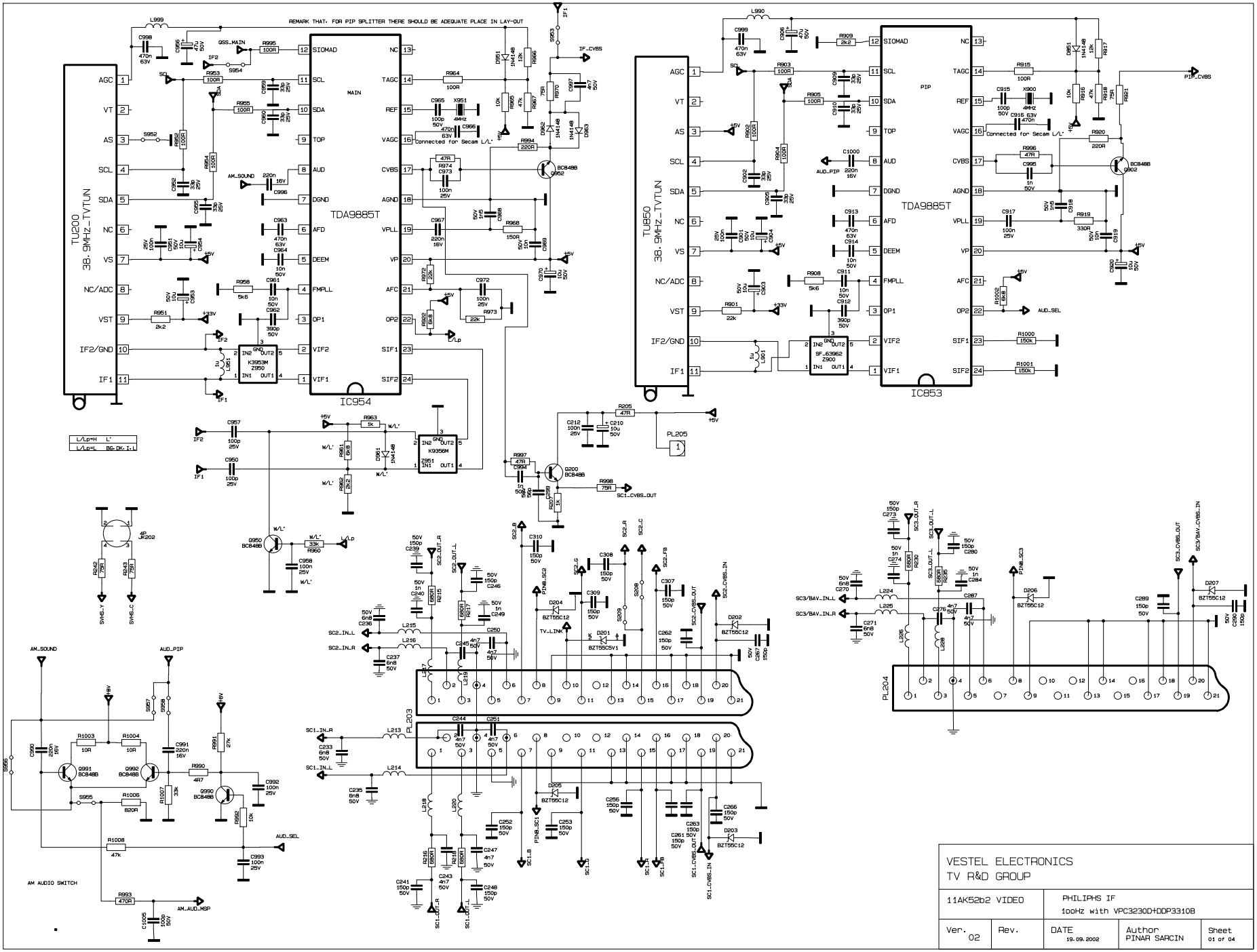
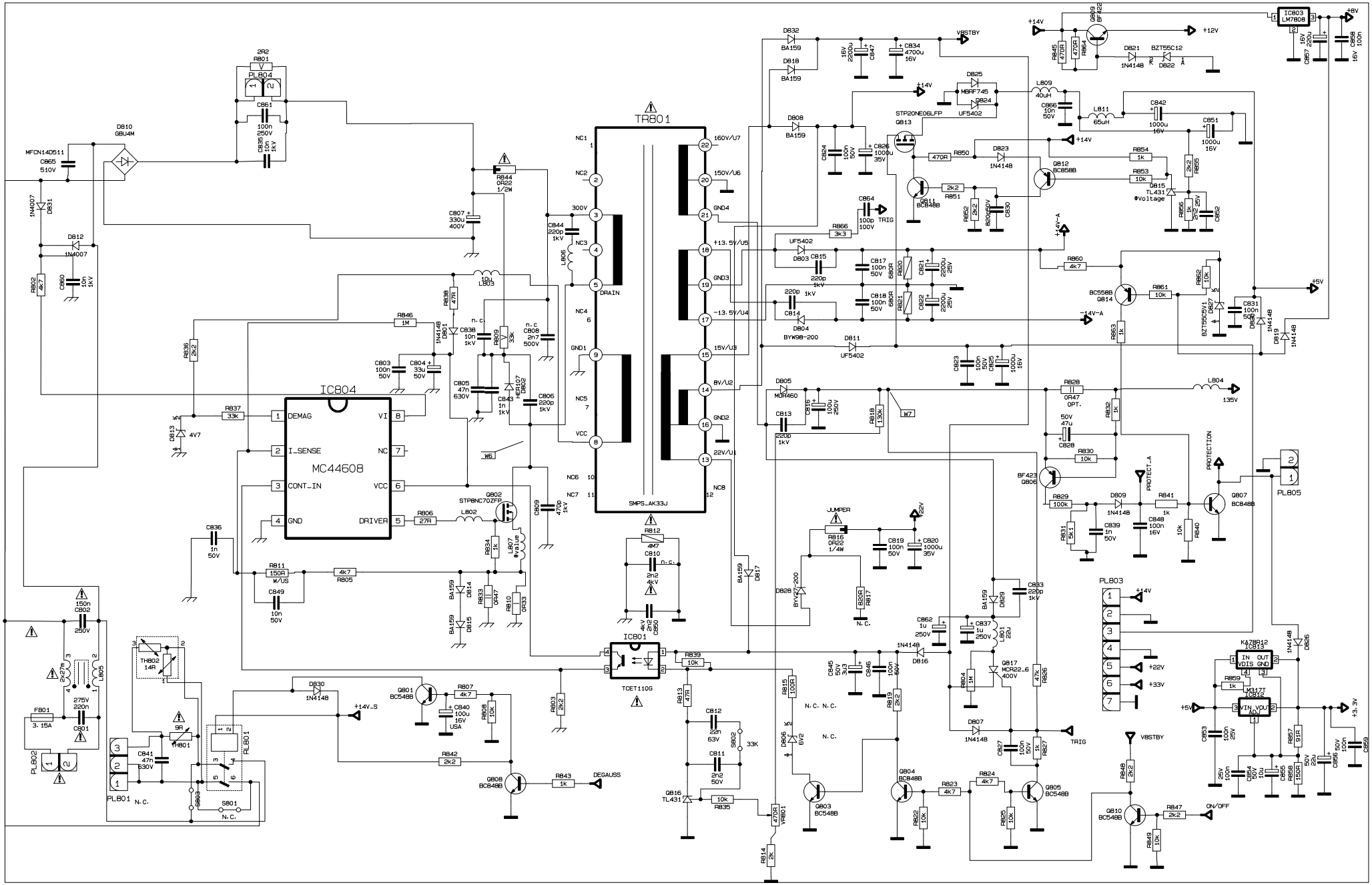
VI
NC
VCC
DRIVER
TR801
SMPS_4K33J
DRAIN
160V/U7
150V/U6
GND4
+13.5V/U5
GND3
-13.5V/U4
15V/U3
8V/U2
GND2
22V/U1
IC801
TCET110G
Q802
STP8NC70ZFP
Q813
STP20NE06LFP
IC803
LM7808
PL803
PL804
PL805
PL801
PL802
JUMPER
W6
W7
MFCN14D511
D810
GBU4M
TH801
TH802
F801
3.15A
S801
N.C.
+14V
+12V
+8V
+5V
+3.3V
+22V
+33V
-14V-A
+14V_S
VBSTBY
TRIG
DEGAUSS
ON/OFF
135V
PROTECTION
PROTECT_A
Voltage
OPT.
IC813
K7805
IC814
M317T
ADJ
IC815
K7812
VDIS
VIN
VOUT
GND


IC100
STV9379FA
INVERT_IN
VCC
FBKSUPPLY
GND
OUT
OUTSUPPLY
N_INVERT_IN
Deflection Conn
IC105
LM358N
OUT1
INVIN1
NONINVIN1
VCC-
VCC+
OUT2
INVIN2
NONINVIN2
TR101
FBT_ELDOR_AK41
COLLECTOR
600V
135V
SUP_VOL
+200V
+50V
HEATER
-11V
GND
E/W
Vert.Sup+
Vert.Sup-
ANODE
GND2
FOCUS1_STATIC
FOCUS2_DYNAMIC
G2
DYN_FCS
ABL
PROTECT_A
+14V
+8V
+210V
+33V
HFLYB
V_fb
ON/OFF
+14V_S
-14V-A
+14V-A
HDRIVE
EW
DAF_VERT
VERT+
VERT-
VFROT
ROTATION
ODD/EVEN
DYN_FOCUS
ROTATION COIL SOCKET
PL107
CRT Board Supply
PL101
11AK52_FBT
NOT:*===TUP DEGISKENLERI
VESTEL ELECTRONICS
TV R&D GROUP
11AK52E-4
PHILIPHS IF
FBT
Ver. 02
Rev. 01
DATE 19.08.2002
Author PINAR SARCIN
Sheet 03 of 04


REMARK THAT: FOR PIP SPLITTER THERE SHOULD BE ADEQUATE PLACE IN LAY-OUT
TU200 38.9MHZ_TVTUN
IC954
TDA9885T
MAIN
TU850 38.9MHZ_TVTUN
IC853
PIP
K3953M 2950
K9356M 7951
SF_63962 2900
AM_SOUND
AUD_PIP
AM AUDIO SWITCH
AM_AUD_MSP
IF_CVBS
PIP_CVBS
AUD_SEL
L/Lp
SC1_CVBS_OUT
VESTEL ELECTRONICS
TV R&D GROUP
11AK52b2 VIDEO
PHILIPHS IF
1ooHz with VPC3230D+DDP3310B
Ver. 02
Rev.
DATE 19.09.2002
Author PINAR SARCIN
Sheet 01 of 04

AK52-B4


IC804
MC44608
DEMAG
I_SENSE
CONT_IN
GND
VI
NC
VCC
DRIVER
TR801
SMPS_AK33J
DRAIN
160V/U7
150V/U6
GND4
+13.5V/U5
GND3
-13.5V/U4
15V/U3
8V/U2
GND2
22V/U1
IC801
TCET110G
Q802
STP8NC70ZFP
Q813
STP20NE06LFP
IC803
LM7808
IC813
KA78R12
IC812
M317T
PL801
PL802
PL803
PL804
PL805
TH801
TH802
S801
JUMPER
PROTECTION
PROTECT_A
ON/OFF
TRIG
DEGAUSS
+14V
+12V
+5V
+3.3V
+22V
+33V
135V
VBSTBY
+14V-A
-14V-A
+14V-S
MFCN14D511
GBU4M
BZT55C12
BZT55C5V1
TL431
BC548B
BC558B
BC848B
BF422
BF423
MBRF745
UF5402
BYW98-200
BYV27-200
MUR460
MCR22-6
1N4148
1N4007
BA159
W1
W2
W3
W4
W5
W6
W7
W8
W9
W10
W11
W12
W13
W14
W15
W16
W17
W18
W19
W20
W21
W22
W23
W24
W25
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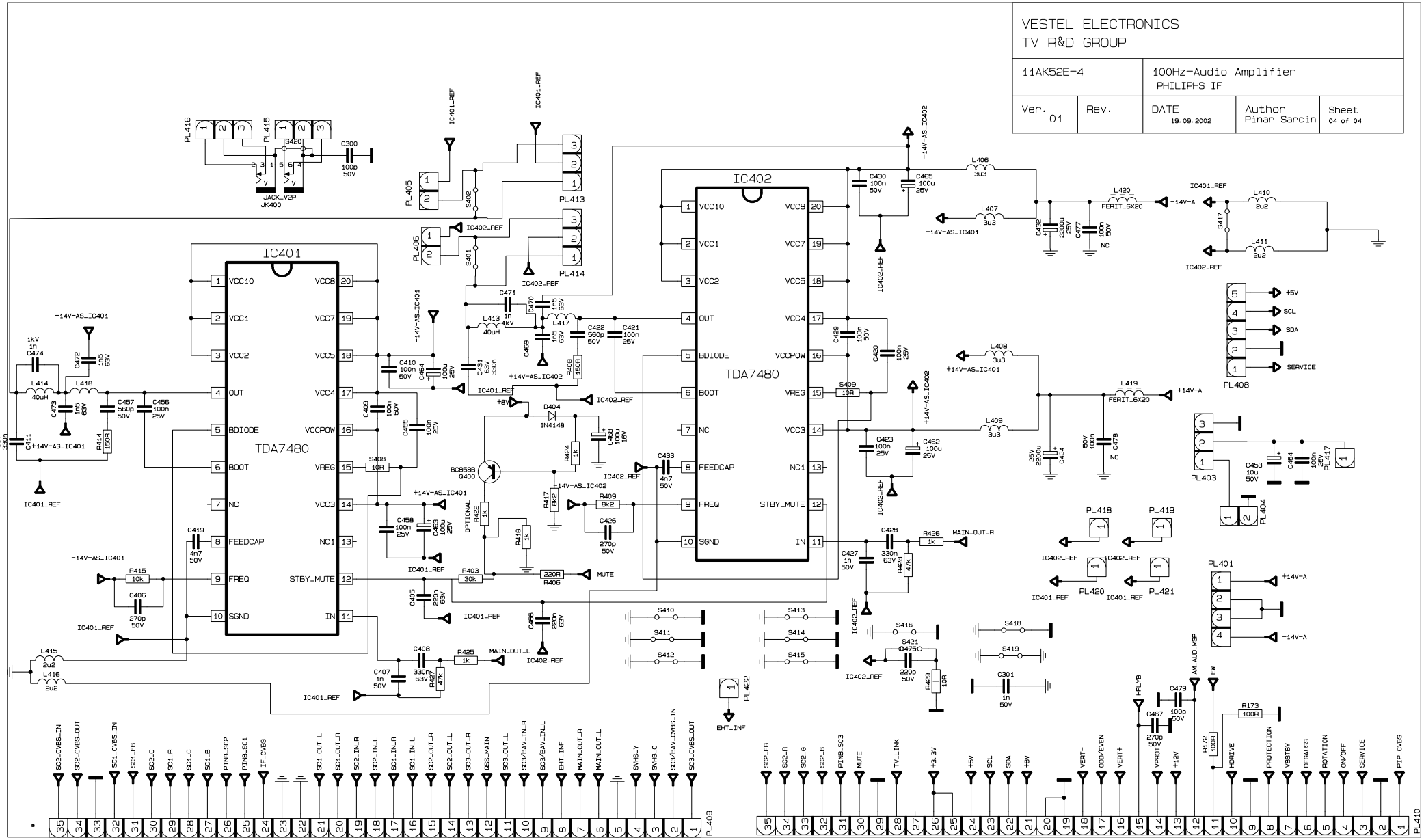
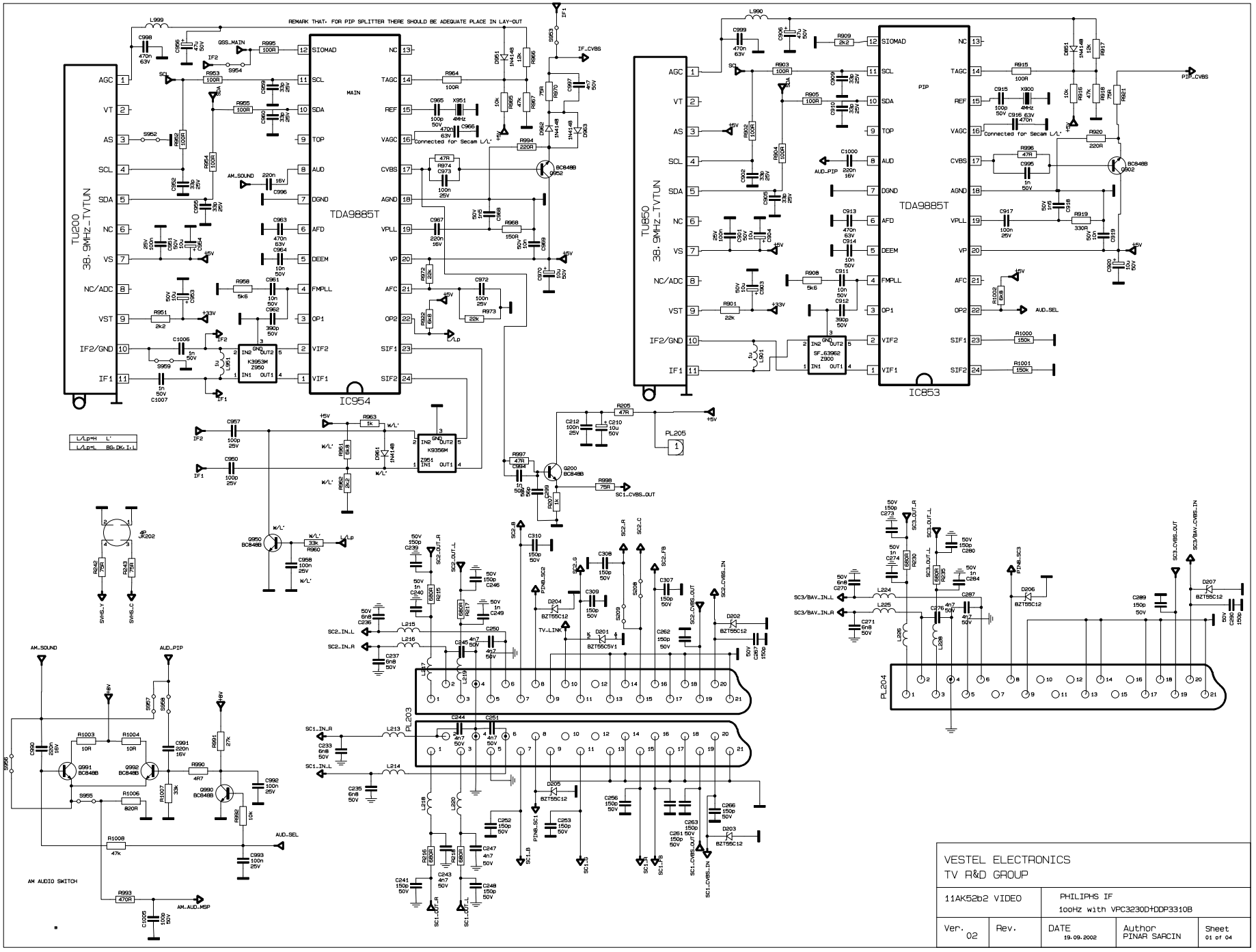
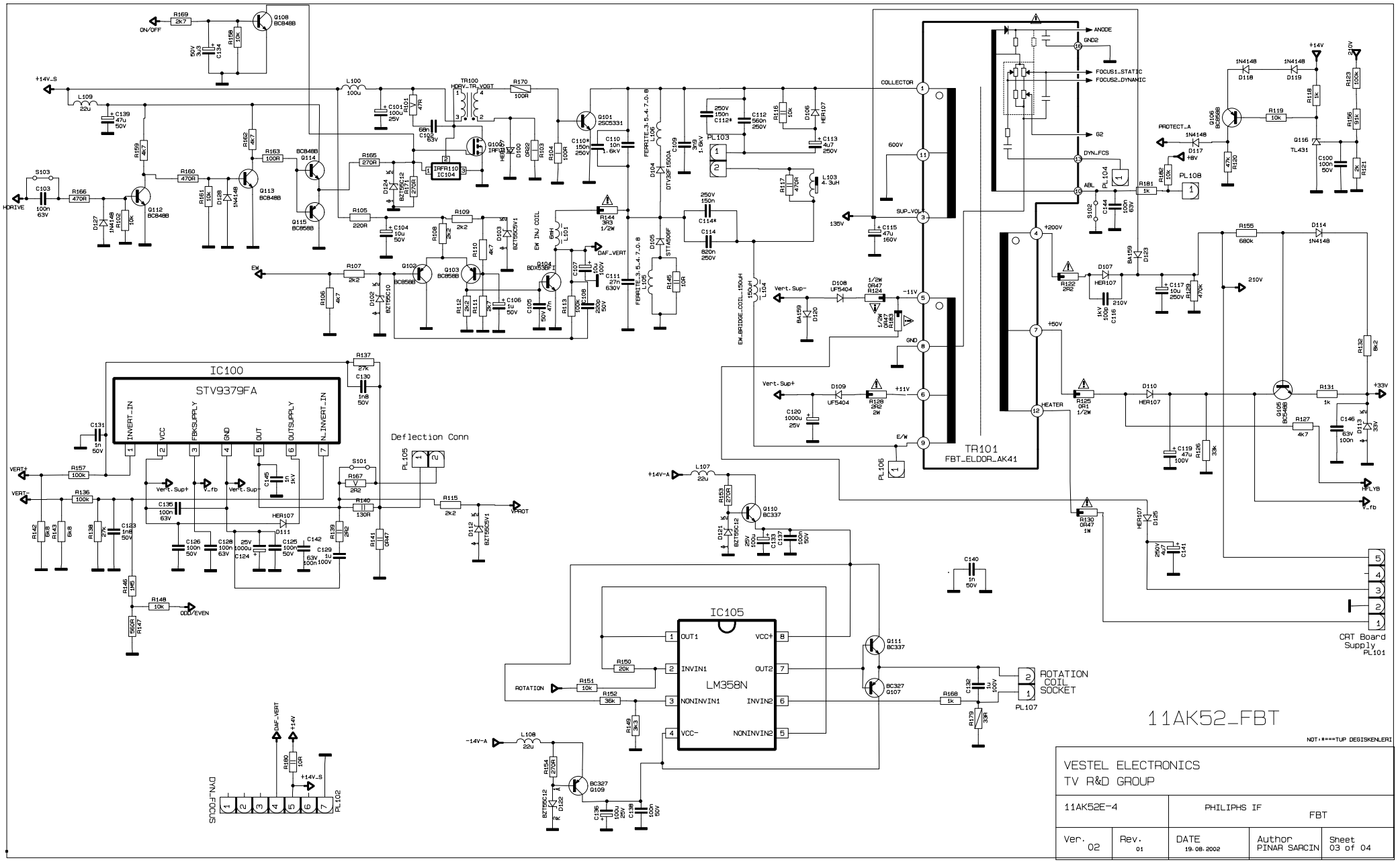
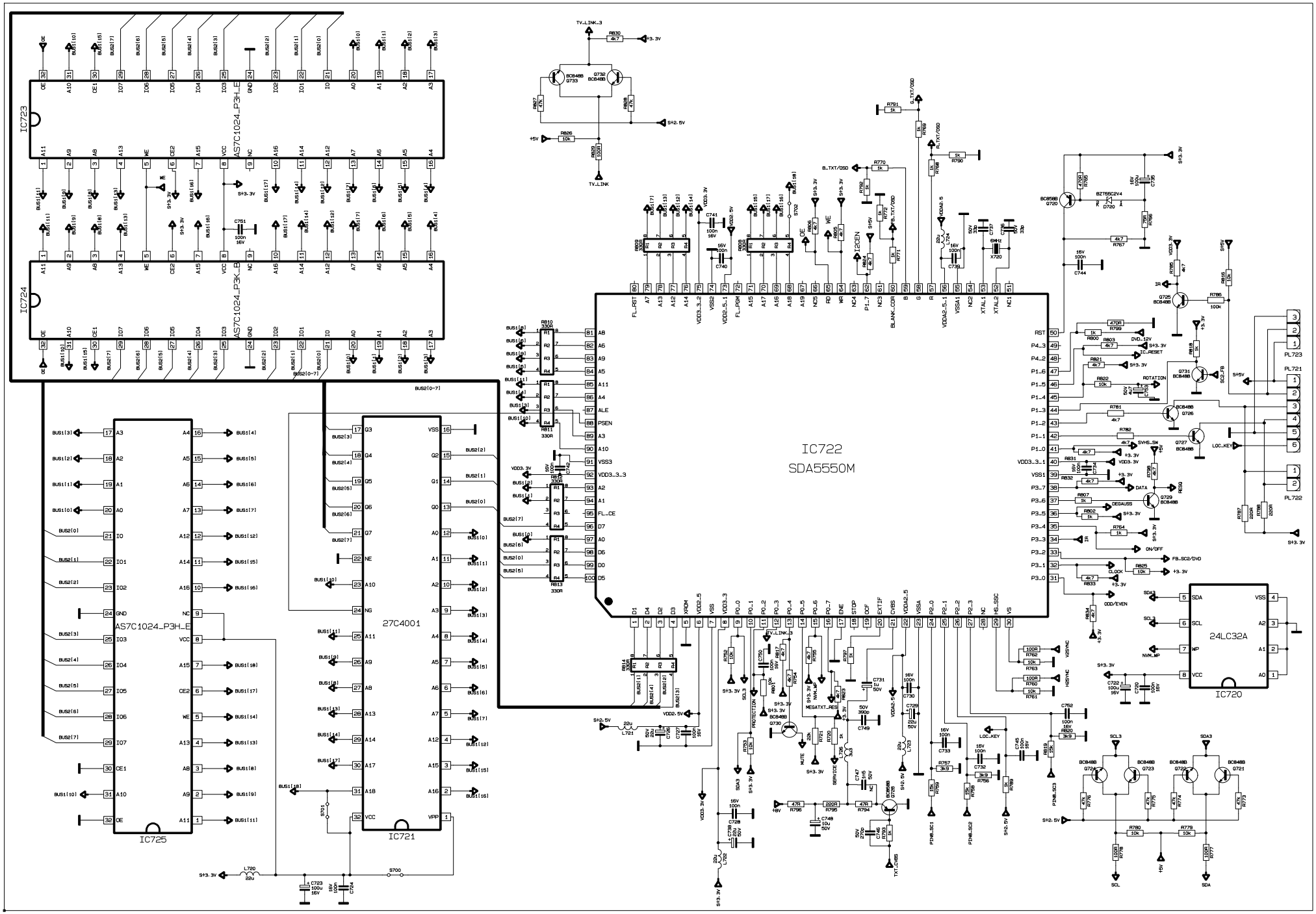
W37
W38
W39
W40


VESTEL ELECTRONICS
TV R&D GROUP
11AK52E-4
100Hz-Audio Amplifier
PHILIPHS IF
Ver. 01
Rev.
DATE 19.09.2002
Author Pinar Sarcin
Sheet 04 of 04
IC401
IC402
TDA7480
VCC10
VCC1
VCC2
OUT
BDIODE
BOOT
NC
FEEDCAP
FREQ
SGND
VCC8
VCC7
VCC5
VCC4
VCCPOW
VREG
VCC3
NC1
STBY_MUTE
IN
-14V-AS_IC401
-14V-AS_IC402
+14V-AS_IC401
+14V-AS_IC402
IC401_REF
IC402_REF
+8V
MUTE
MAIN_OUT_L
MAIN_OUT_R
OPTIONAL
BC858B Q400
D404 1N4148
PL405
PL406
PL413
PL414
PL415
PL416
JACK_V2P JK400
S402
S401
S420
PL408
PL403
PL404
PL417
PL418
PL419
PL420
PL421
PL401
PL422
EHT_INF
PL409
PL410
SC2_CVBS_IN
SC2_CVBS_OUT
SC1_CVBS_IN
SC1_FB
SC2_C
SC1_R
SC1_G
SC1_B
PIN8_SC2
PIN8_SC1
IF_CVBS
SC1_OUT_L
SC1_OUT_R
SC2_IN_R
SC2_IN_L
SC1_IN_R
SC1_IN_L
SC2_OUT_R
SC2_OUT_L
SC3_OUT_R
QSS_MAIN
SC3_OUT_L
SC3/BAV_IN_R
SC3/BAV_IN_L
EHT_INF
MAIN_OUT_R
MAIN_OUT_L
SVHS_Y
SVHS_C
SC3/BAV_CVBS_IN
SC3_CVBS_OUT
SC2_FB
SC2_R
SC2_G
SC2_B
PIN8_SC3
MUTE
TV_LINK
+3.3V
+5V
SCL
SDA
+8V
VERT-
ODD/EVEN
VERT+
VPROT
+12V
AM_AUD_MSP
EW
HFLYB
HDRIVE
PROTECTION
VBSTBY
DEGAUSS
ROTATION
ON/OFF
SERVICE
PIP_CVBS
+5V
SCL
SDA
SERVICE
+14V-A
-14V-A


REMARK THAT, FOR PIP SPLITTER THERE SHOULD BE ADEQUATE PLACE IN LAY-OUT
TU200
38.9MHz_TVTUN
TDA9885T
MAIN
IC954
TU850
38.9MHz_TVTUN
TDA9885T
PIP
IC853
AGC
VT
AS
SCL
SDA
NC
VS
NC/ADC
VST
IF2/GND
IF1
SIOMAD
TOP
AUD
DGND
AFD
DEEM
FMPLL
OP1
OP2
VIF2
VIF1
NC
REF
VAGC
CVBS
AGND
VPLL
VP
AFC
SIF1
SIF2
TAGC
IF_CVBS
PIP_CVBS
AUD_PIP
AUD_SEL
AM_SOUND
AUD_PIP
AUD_SEL
AM AUDIO SWITCH
AM_AUD_MSP
SC2_IN_L
SC2_IN_R
SC1_IN_L
SC1_IN_R
SC2_CVBS_OUT
SC2_CVBS_IN
SC1_CVBS_OUT
SC1_CVBS_IN
SC3/BAV_IN_L
SC3/BAV_IN_R
SC3_CVBS_OUT
SC3/BAV_CVBS_IN
TV_LINK
PIN8_SC2
PIN8_SC1
PIN8_SC3
PL203
PL204
PL205
VESTEL ELECTRONICS
TV R&D GROUP
11AK52b2 VIDEO
PHILIPHS IF
100Hz with VPC3230D+DDP3310B
Ver. 02
Rev.
DATE 19.09.2002
Author PINAR SARCIN
Sheet 01 of 04


IC100
STV9379FA
INVERT_IN
VCC
FBKSUPPLY
GND
OUT
OUTSUPPLY
N_INVERT_IN
Deflection Conn
IC105
LM358N
OUT1
INVIN1
NONINVIN1
VCC-
VCC+
OUT2
INVIN2
NONINVIN2
TR101
FBT_ELDOR_AK41
COLLECTOR
600V
135V
SUP_VOL
+200V
+50V
HEATER
-11V
GND
E/W
Vert.Sup+
Vert.Sup-
ANODE
GND2
FOCUS1_STATIC
FOCUS2_DYNAMIC
G2
DYN_FCS
ABL
PROTECT_A
+14V
+8V
210V
+33V
HFLYB
V_fb
EW
DAF_VERT
VERT+
VERT-
VERROT
ON/OFF
HDRIVE
ROTATION
ODD/EVEN
DYN_FOCUS
CRT Board Supply PL101
ROTATION COIL SOCKET
PL107
11AK52_FBT
NOT:*===TUP DEGISKENLERI
VESTEL ELECTRONICS
TV R&D GROUP
11AK52E-4
PHILIPHS IF
FBT
Ver. 02
Rev. 01
DATE 19.08.2002
Author PINAR SARCIN
Sheet 03 of 04

FB52-A1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IC723
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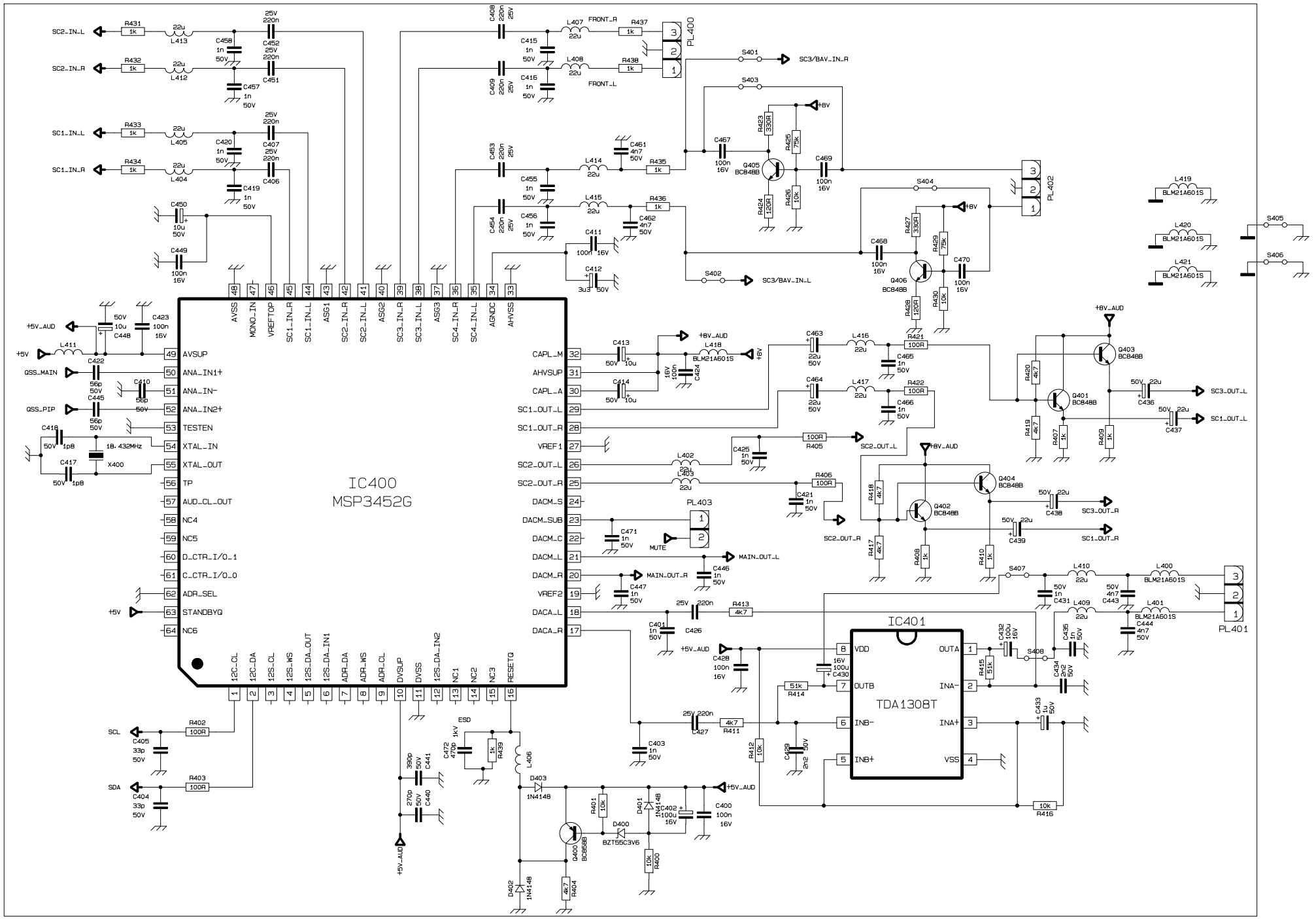
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PL400
PL401
PL402
PL403
SC2_IN_L
SC2_IN_R
SC1_IN_L
SC1_IN_R
FRONT_R
FRONT_L
SC3/BAV_IN_R
SC3/BAV_IN_L
+8V
+8V_AUD
+5V_AUD
+5V
QSS_MAIN
QSS_PIP
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MUTE
MAIN_OUT_L
MAIN_OUT_R
SC2_OUT_L
SC2_OUT_R
SC3_OUT_L
SC1_OUT_L
SC3_OUT_R
SC1_OUT_R
SCL
SDA
ESD
AVSS
MONO_IN
VREFTOP
SC1_IN_R
SC1_IN_L
ASG1
SC2_IN_R
SC2_IN_L
ASG2
SC3_IN_R
SC3_IN_L
ASG3
SC4_IN_R
SC4_IN_L
AGNDC
AHVSS
AVSUP
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ANA_IN-
ANA_IN2+
TESTEN
XTAL_IN
XTAL_OUT
TP
AUD_CL_OUT
NC4
NC5
D_CTR_I/O_1
C_CTR_I/O_0
ADR_SEL
STANDBYQ
NC6
CAPL_M
AHVSUP
CAPL_A
SC1_OUT_L
SC1_OUT_R
VREF1
SC2_OUT_L
SC2_OUT_R
DACM_S
DACM_SUB
DACM_C
DACM_L
DACM_R
VREF2
DACA_L
DACA_R
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I2C_DA
I2S_CL
I2S_WS
I2S_DA_OUT
I2S_DA_IN1
ADR_DA
ADR_WS
ADR_CL
DVSUP
DVSS
I2S_DA_IN2
NC1
NC2
NC3
RESETQ
VDD
OUTA
OUTB
INA-
INB-
INA+
INB+
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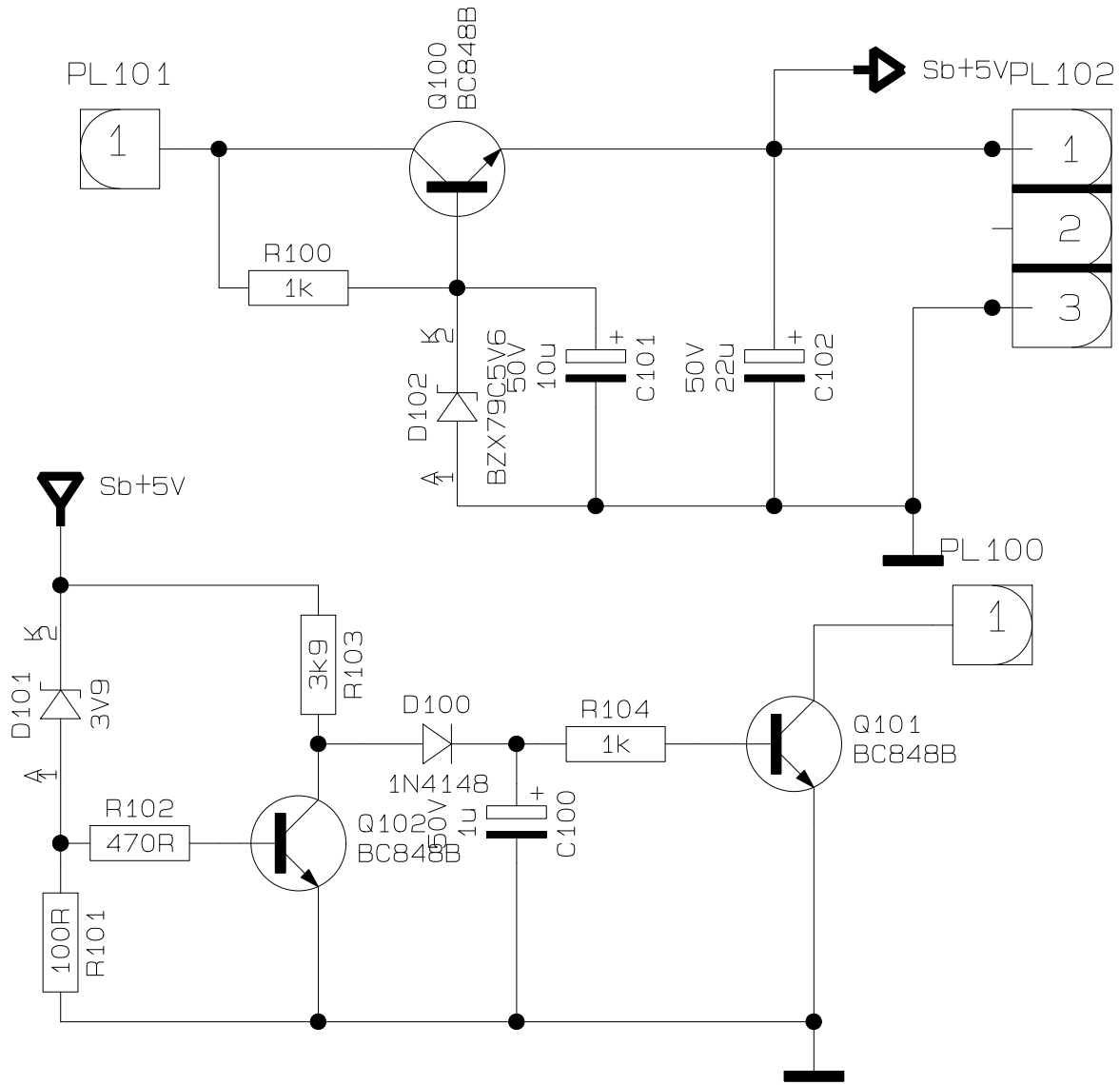
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Sb+5V
PL102
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2
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R100
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D102
BZX79C5V6
K
A
50V
10u
C101
50V
22u
C102
Sb+5V
PL100
1
D101
3V9
K
A
3k9
R103
D100
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R102
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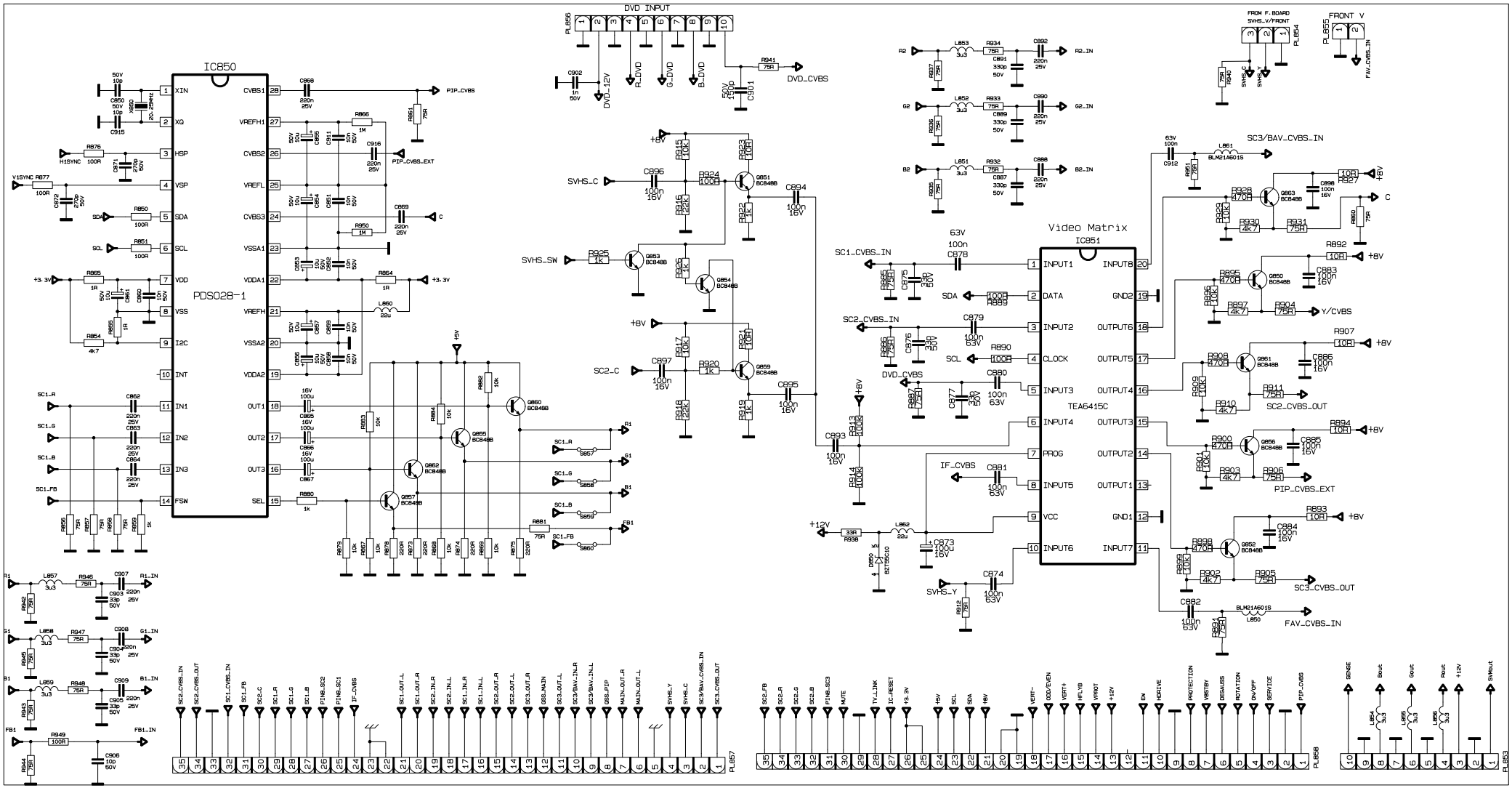
C100
100R
R101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VREFH1
CVBS2
VREFL
CVBS3
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VREFH
VSSA2
VDDA2
OUT1
OUT2
OUT3
SEL
DVD INPUT
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DVD_CVBS
PIP_CVBS
PIP_CVBS_EXT
SVHS_C
SVHS_SW
SC2_C
Video Matrix
IC851
TEA6415C
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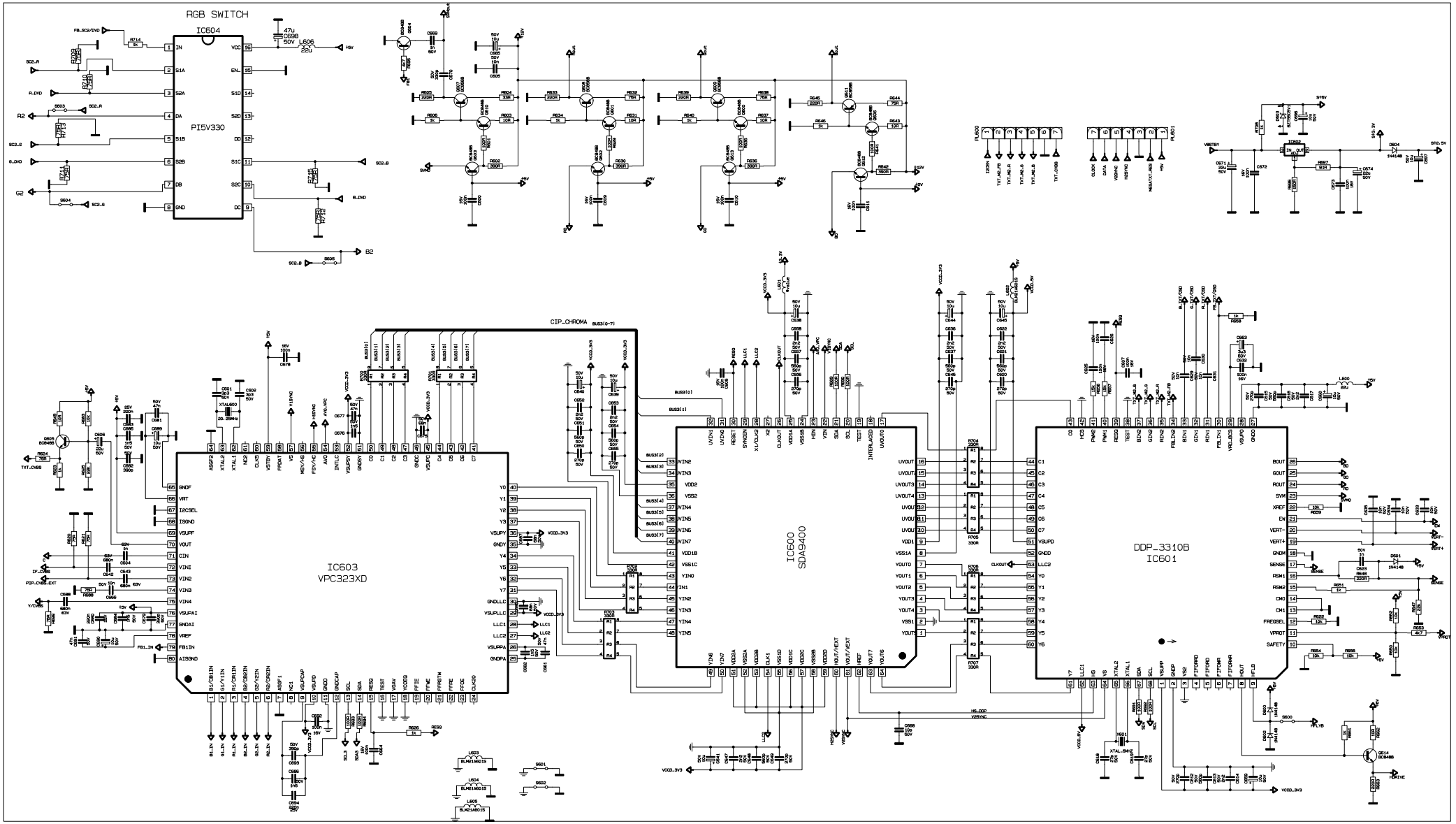
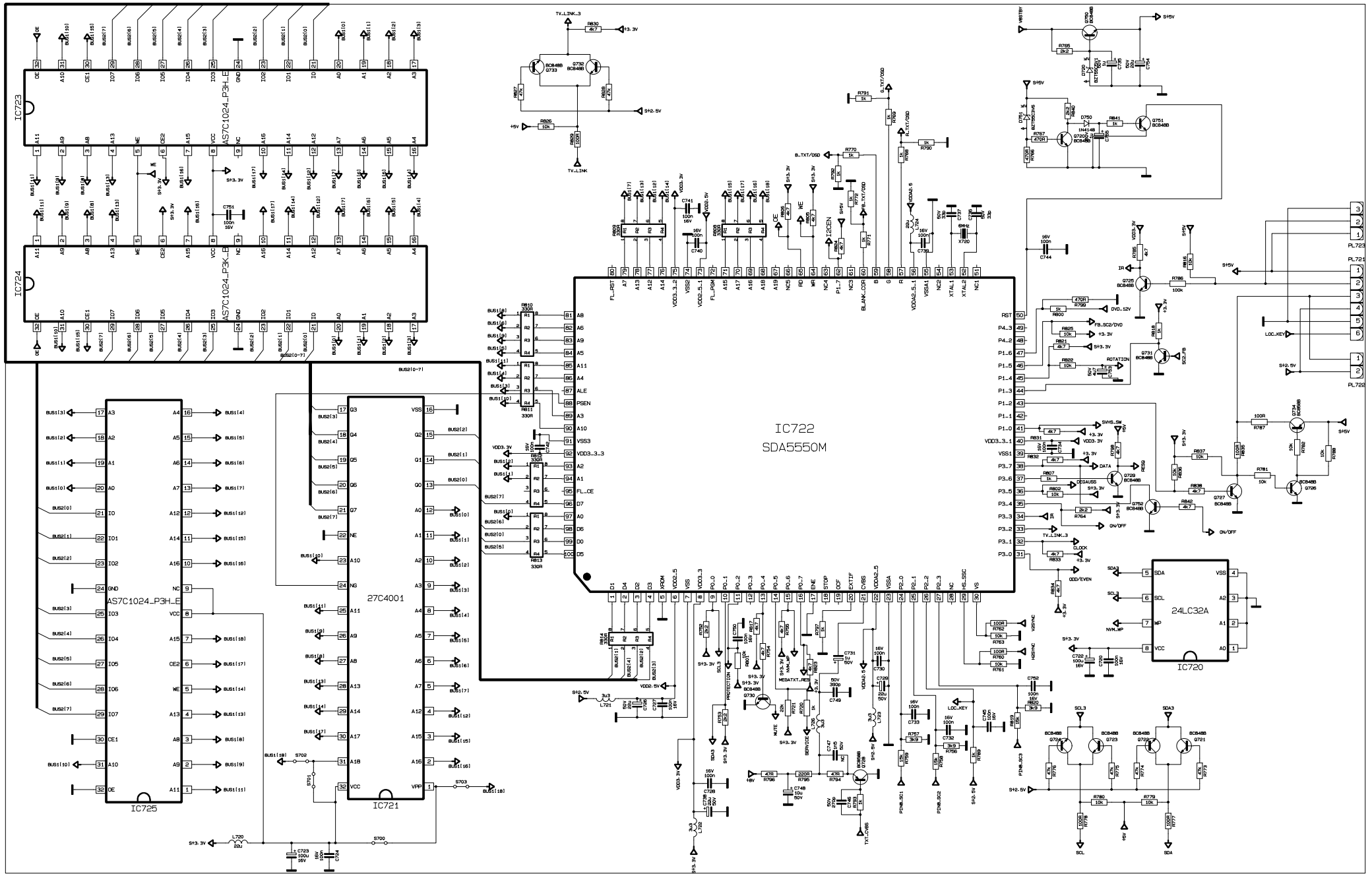
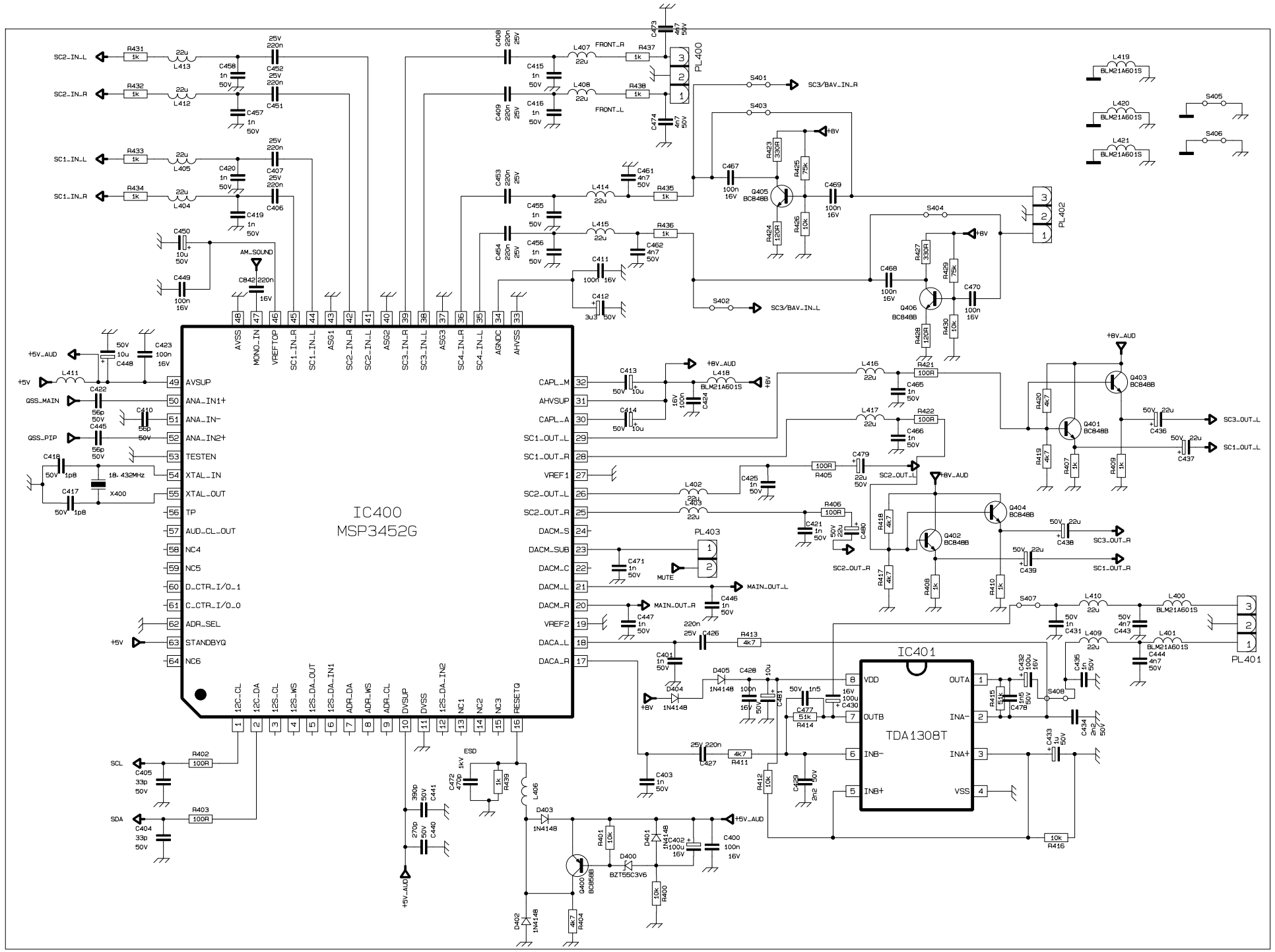
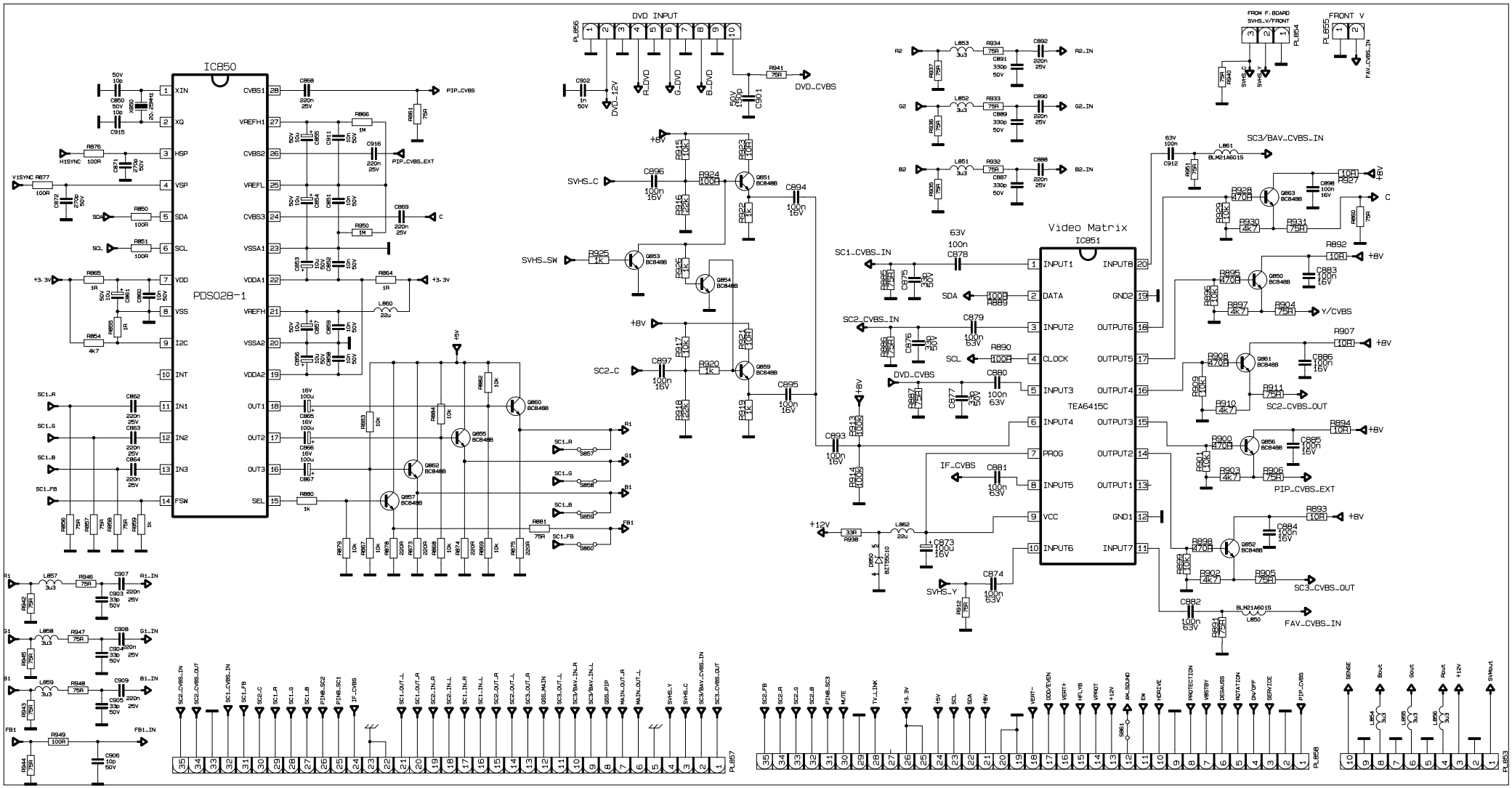
INPUT2
INPUT3
INPUT4
INPUT5
INPUT6
INPUT7
INPUT8
PROG
VCC
GND1
GND2
OUTPUT1
OUTPUT2
OUTPUT3
OUTPUT4
OUTPUT5
OUTPUT6
DATA
CLOCK
SC1_CVBS_IN
SC2_CVBS_IN
IF_CVBS
SVHS_Y
FRONT V
FAV_CVBS_IN
SC3/BAV_CVBS_IN
Y/CVBS
SC2_CVBS_OUT
PIP_CVBS_EXT
SC3_CVBS_OUT
FAV_CVBS_IN
PL857
PL858
PL853

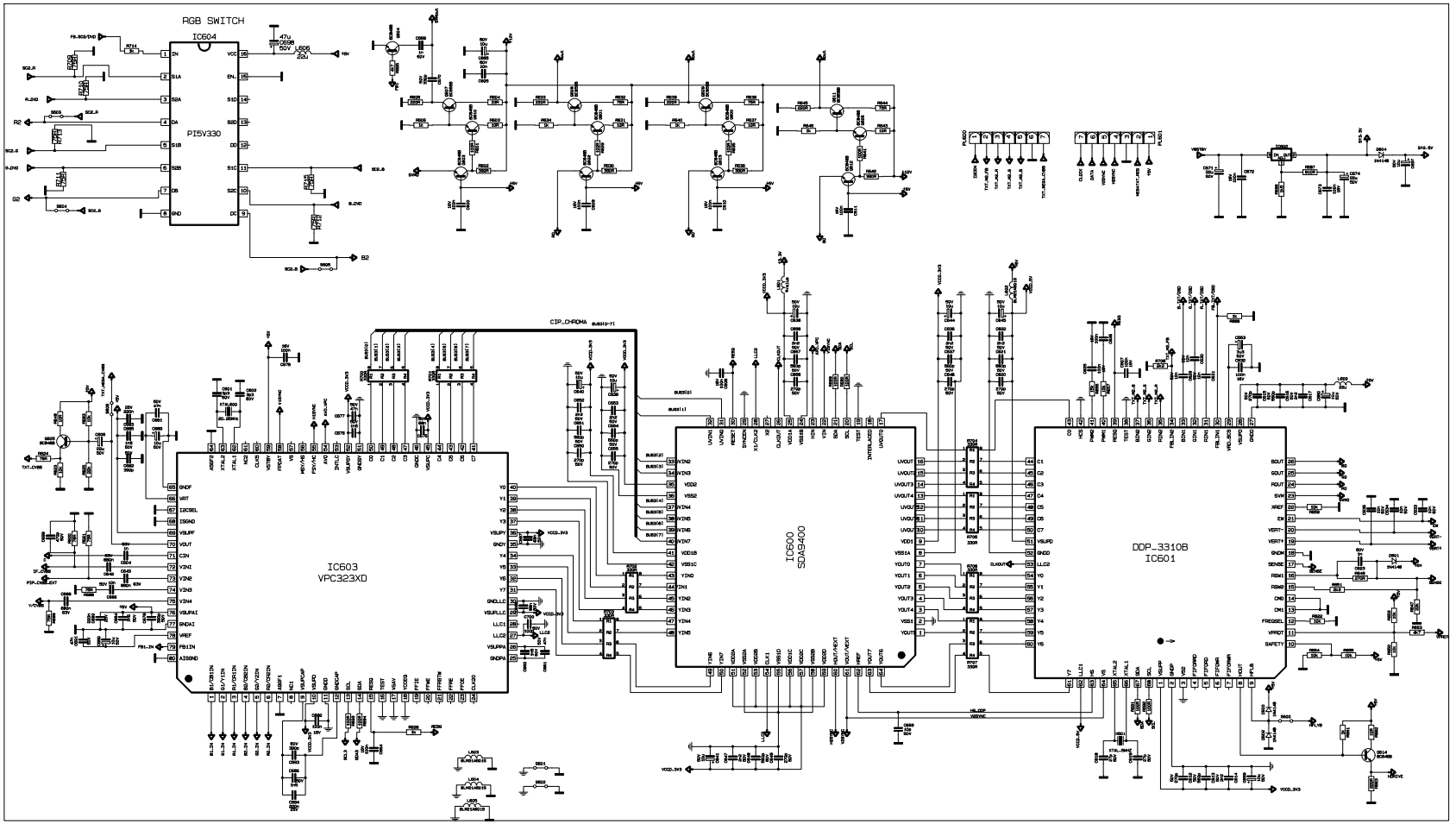

RGB SWITCH
IC604
PI5V330
IC603
VPC323XD
IC600
SDA9400
DDP_3310B
IC601
CIP_CHROMA
BUS3[0-7]
HS_DDP
VSYNC

FB52-A3

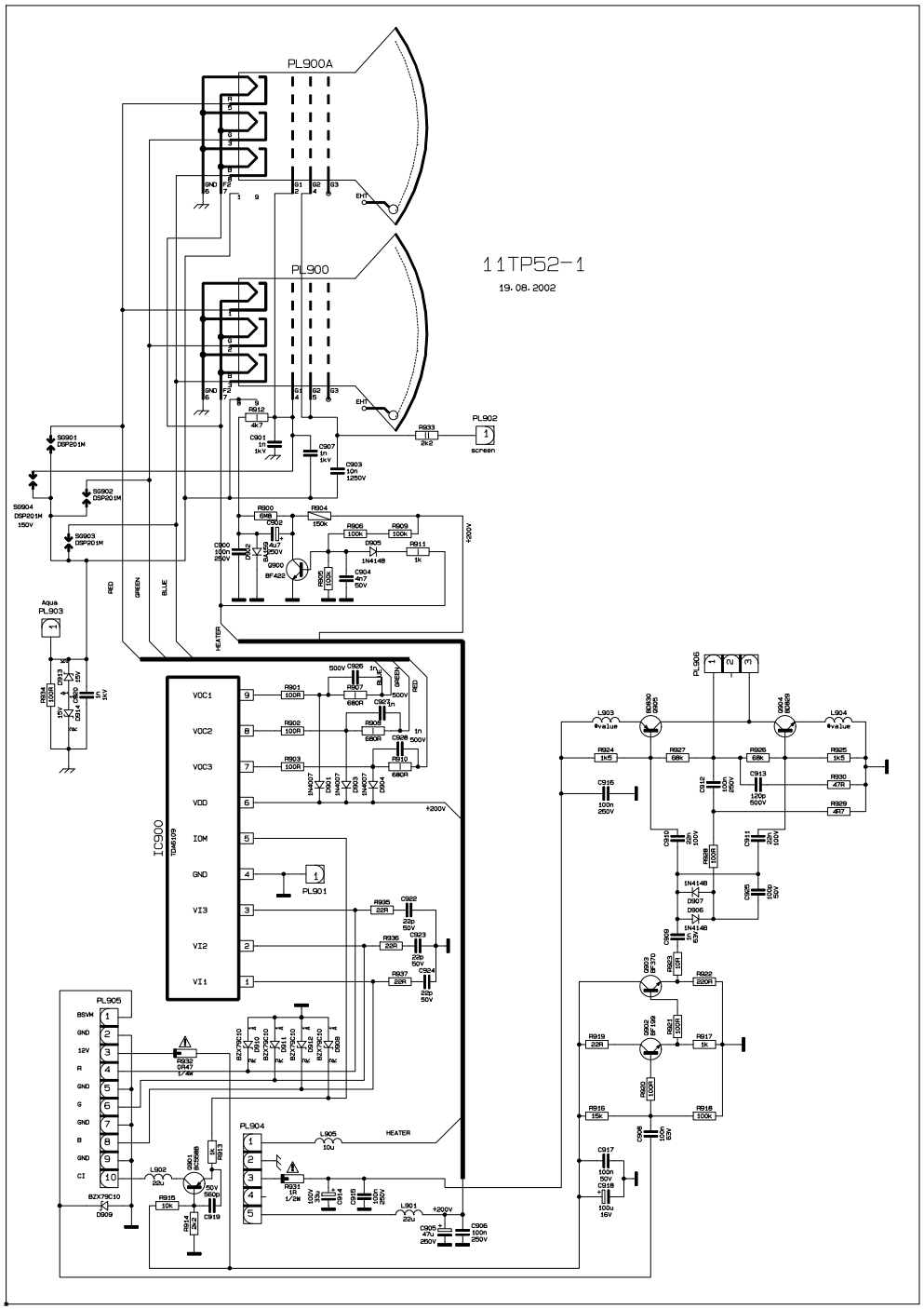

IC722
SDA5550M
IC723
AS7C1024_P3H_E
IC724
AS7C1024_P3K_E
IC725
AS7C1024_P3H_E
IC721
27C4001
IC720
24LC32A
PL721
PL722
PL723
TV_LINK_3
TV_LINK
FL_RST
FL_PSM
FL_CE
BLANK_CCR
TXT/OSD
R_TXT/OSD
B_TXT/OSD
I2CEN
OE
WE
RST
DATA
CLOCK
ON/OFF
ROTATION
LOC_KEY
MESATXT_RES
PROTECTION
SCL3
SDA3
VDD3_3V
VDD2_5V
S+3.3V
S+5V
S+12.5V
S+8.5V


IC400
MSP3452G
IC401
TDA1308T
PL400
PL401
PL402
PL403
SC2_IN_L
SC2_IN_R
SC1_IN_L
SC1_IN_R
AM_SOUND
FRONT_R
FRONT_L
SC3/BAV_IN_R
SC3/BAV_IN_L
+8V
+8V_AUD
+5V_AUD
+5V
QSS_MAIN
QSS_PIP
18.432MHz
X400
MUTE
MAIN_OUT_L
MAIN_OUT_R
SC2_OUT_L
SC2_OUT_R
SC3_OUT_L
SC3_OUT_R
SC1_OUT_L
SC1_OUT_R
SCL
SDA
ESD
STANDBYQ
ADR_SEL
AVSUP
ANA_IN1+
ANA_IN-
ANA_IN2+
TESTEN
XTAL_IN
XTAL_OUT
TP
AUD_CL_OUT
NC4
NC5
D_CTR_I/O_1
C_CTR_I/O_0
NC6
CAPL_M
AHVSUP
CAPL_A
VREF1
VREF2
DACM_S
DACM_SUB
DACM_C
DACM_L
DACM_R
DACA_L
DACA_R
I2C_CL
I2C_DA
I2S_CL
I2S_WS
I2S_DA_OUT
I2S_DA_IN1
ADR_DA
ADR_WS
ADR_CL
DVSUP
DVSS
I2S_DA_IN2
NC1
NC2
NC3
RESETQ
AVSS
MONO_IN
VREFTOP
SC1_IN_R
SC1_IN_L
ASG1
SC2_IN_R
SC2_IN_L
ASG2
SC3_IN_R
SC3_IN_L
ASG3
SC4_IN_R
SC4_IN_L
AGNDC
AHVSS
VDD
OUTA
OUTB
INA-
INB-
INA+
INB+
VSS

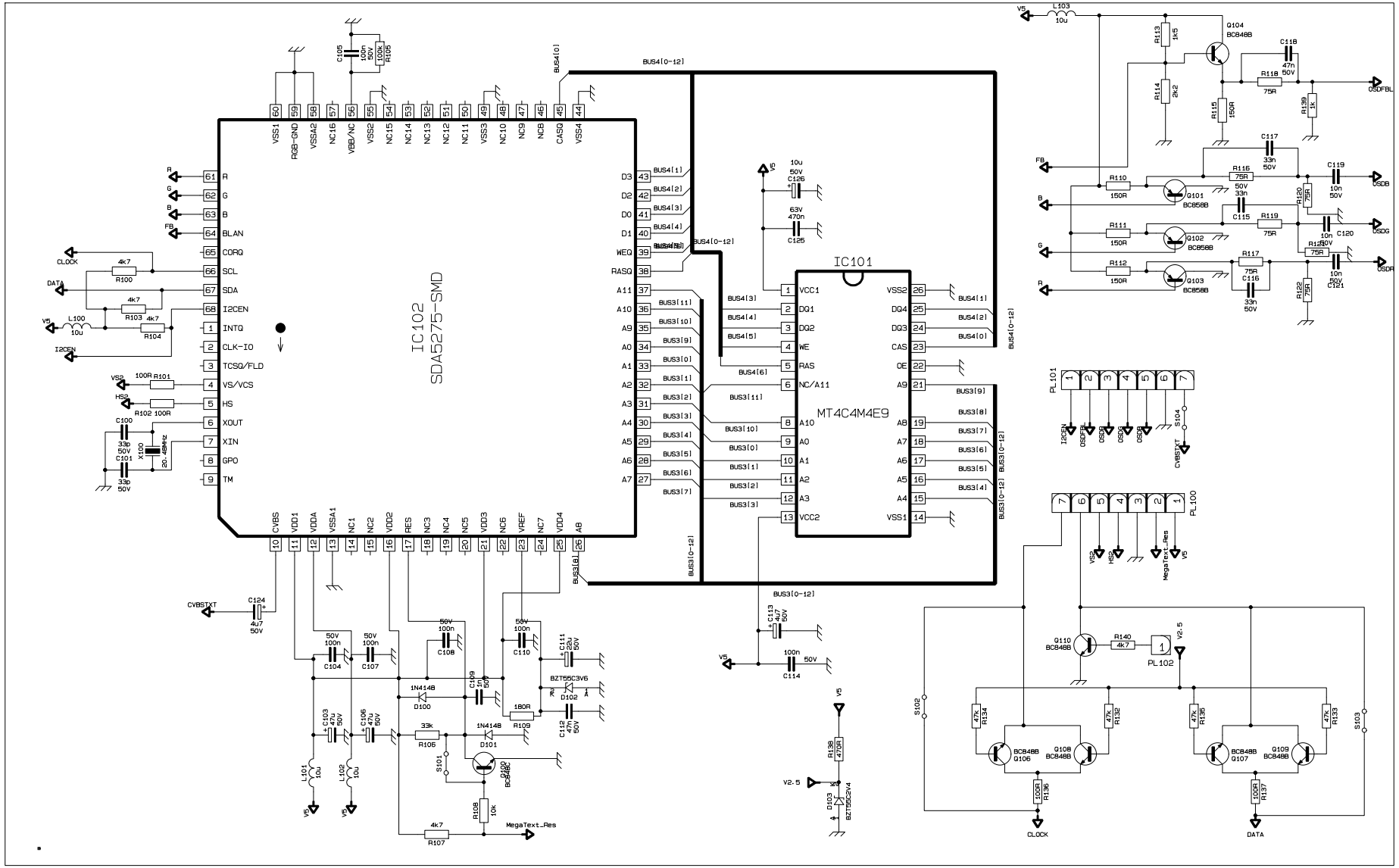

IC850
PDS028-1
XIN
XO
HSP
VSP
SDA
SCL
VDD
VSS
I2C
INT
IN1
IN2
IN3
FSW
CVBS1
VREFH1
CVBS2
VREFL
CVBS3
VSSA1
VDDA1
VREFH
VSSA2
VDDA2
OUT1
OUT2
OUT3
SEL
DVD INPUT
DVD_CVBS
PIP_CVBS
PIP_CVBS_EXT
SVHS_C
SVHS_SW
SC2_C
Video Matrix
IC851
TEA6415C
INPUT1
INPUT2
INPUT3
INPUT4
INPUT5
INPUT6
INPUT7
INPUT8
DATA
CLOCK
PROG
VCC
GND1
GND2
OUTPUT1
OUTPUT2
OUTPUT3
OUTPUT4
OUTPUT5
OUTPUT6
SC1_CVBS_IN
SC2_CVBS_IN
IF_CVBS
SVHS_Y
SC3/BAV_CVBS_IN
Y/CVBS
SC2_CVBS_OUT
PIP_CVBS_EXT
SC3_CVBS_OUT
FAV_CVBS_IN
FRONT V
FROM F.BOARD
SVHS_V/FRONT
R2_IN
G2_IN
B2_IN
R1_IN
G1_IN
B1_IN
FB1_IN
SC1_R
SC1_G
SC1_B
SC1_FB


RGB SWITCH
IC604
PI5V330
IC603
VPC323XD
IC600
SDA9400
DDP_3310B
IC601

TP52-1


11TP52-1
19.08.2002
PL900A
PL900
PL902
screen
PL903
Aqua
PL901
PL904
PL905
PL906
IC900
TDA4109
VOC1
VOC2
VOC3
VDD
IOM
GND
VI3
VI2
VI1
HEATER
RED
GREEN
BLUE
+200V
EHT
S9901 DSP201M
S9902 DSP201M
S9903 DSP201M
S9904 DSP201M 150V

TXT52


IC102
SDA5275-SMD
IC101
MT4C4M4E9
R
G
B
BLAN
CORQ
SCL
SDA
I2CEN
INTQ
CLK-IO
TCSQ/FLD
VS/VCS
HS
XOUT
XIN
GPO
TM
CVBS
VDD1
VDDA
VSSA1
NC1
NC2
VDD2
RES
NC3
NC4
NC5
VDD3
NC6
VREF
NC7
VDD4
AB
VSS1
RGB-GND
VSSA2
NC16
VBB/NC
VSS2
NC15
NC14
NC13
NC12
NC11
VSS3
NC10
NC9
NCB
CASQ
VSS4
D3
D2
D0
D1
WEQ
RASQ
A11
A10
A9
A0
A1
A2
A3
A4
A5
A6
A7
BUS4[0-12]
BUS3[0-12]
CLOCK
DATA
I2CEN
CVBSTXT
MegaText_Res
OSDFBL
OSDB
OSDG
OSDR
CLOCK
DATA

Parts List

BILL OF MATERIAL LIST

10020021 2841 TOSHIBA TOSHIBA 28H37GZ(AK52)

NO	PART NUMBER	DESCRIPTION	UNIT	QTY	POSITION NUMBER				
1	V20000586	SPK.A.28"-32"(16:9)/72XX/74XX w/FER(W/HE	PC	1,000	.	.	.	.	.
2	V20039751	SPK.AS.7289/99 721X/20/70/71 (L)19 W/HE	PC	1,000	.	.	.	.	.
3	V30000426	CAP EL 6.8UF 50V M (BPL)	PC	1,000	.	.	.	.	.
4	V30001946	SPEAKER 8R 15W 57*160	PC	1,000	.	.	.	.	.
5	V30001947	TWEETER 8R 15W CLOSED	PC	1,000	.	.	.	.	.
6	V30002238	CABL 2P/200 SPK DIS UL1672AWG24	PC	1,000	.	.	.	.	.
7	V30012632	CNAS 2P/690 DIS W/C+FER UL2547 AWG24	PC	1,000	.	.	.	.	.
8	V50011720	LABEL HIGH END	PC	1,000	.	.	.	.	.
9	V20039752	SPK.AS.7289/99 721X/20/70/71 (R)19 W/HE	PC	1,000	.	.	.	.	.
10	V30000426	CAP EL 6.8UF 50V M (BPL)	PC	1,000	.	.	.	.	.
11	V30001946	SPEAKER 8R 15W 57*160	PC	1,000	.	.	.	.	.
12	V30001947	TWEETER 8R 15W CLOSED	PC	1,000	.	.	.	.	.
13	V30002238	CABL 2P/200 SPK DIS UL1672AWG24	PC	1,000	.	.	.	.	.
14	V30012631	CNAS 2P/760 DIS W/BL C+FER UL2547 AWG24	PC	1,000	.	.	.	.	.
15	V50011720	LABEL HIGH END	PC	1,000	.	.	.	.	.
16	V20085192	ON/OFF SW ASSY.19Y FTZ(TOSHIBA)25-28"4:3	PC	1,000	.	.	.	.	.
17	V30002174	SWITCH ON/OFF 4A/64A	PC	1,000	.	.	.	.	.
18	V30002368	CNAS 2P/650 AC MAINS W/C	PC	1,000	.	.	.	.	.
19	V30016513	POWER CORD 2.2MT JVC (W/FILTER)	PC	1,000	.	.	.	.	.
20	V40000127	SWITCH INSULATION DOOR LK101	PC	1,000	.	.	.	.	.
21	V40001898	MACARON (12cm.lsý ile daralan)	PC	1,000	.	.	.	.	.
22	V20095506	BASE 2840-41-42 (I)28"(4:3) WO/TESLA TÜP	PC	1,000	.	.	.	.	.
23	V60000008	HIPS (NATURAL)	KG	0,838	.	.	.	.	.
24	V60000022	MASTERBATCH (BLACK)	KG	0,004	.	.	.	.	.
25	V20097393	SNOW BOX ASSY 284X 4:3	PC	1,000	.	.	.	.	.
26	V20095507	SNOW BOX TOP 284X	PC	1,000	.	.	.	.	.
27	V60000011	EPS	KG	0,549	.	.	.	.	.
28	V20095508	SNOW BOX BOTTOM 284X	PC	1,000	.	.	.	.	.
29	V60000011	EPS	KG	0,549	.	.	.	.	.
30	V20097395	BUTTON ASSY 2841-2841W-3241W-2441W	PC	1,000	.	.	.	.	.
31	V20094339	BUTTON ON/OFF XX41 (I)	PC	1,000	.	.	.	.	.
32	V60000003	ABS BLACK	KG	0,005	.	.	.	.	.
33	V20094340	BUTTON FUNCTION XX41 (I)	PC	1,000	.	.	.	.	.
34	V60000003	ABS BLACK	KG	0,020	.	.	.	.	.
35	V20094341	LENS LED XX41 (I) MILKY	PC	1,000	.	.	.	.	.
36	V60000008	HIPS (NATURAL)	G	0,014	.	.	.	.	.
37	V60000927	CRYSTAL PS (NATURAL)	G	7,000	.	.	.	.	.
38	V20094352	LENS PRE-AMP XX41 (I)	PC	1,000	.	.	.	.	.
39	V60000927	CRYSTAL PS (NATURAL)	G	0,002	.	.	.	.	.
40	V20108360	BUTTON FUNCT.XX42/42W/43W/44W EKO.GR(I)#	PC	1,000	.	.	.	.	.
41	V60000001	ABS (NATURAL)	KG	0,018	.	.	.	.	.
42	V60001195	MASTERBATCH EKO.GRAY GR 3216 SE1	G	0,090	.	.	.	.	.
43	V35000013	SPRING ON/OFF SWITCH	PC	1,000	.	.	.	.	.
44	V20108637	CN.ASY.52A-TRFPFC 1,7 A E54 + CONN 2/35	PC	1,000	.	.	.	.	.
45	V30018087	CNAS 2P/350 TRFPFC DIS W/C UL1672AWG22	PC	1,000	.	.	.	.	.
46	V30018270	TRF PFC 1,7A 43MH 170W	PC	1,000	.	.	.	.	.
47	V35000217	SCREW S C SYF YFMB 3.5*9.5	PC	1,000	.	.	.	.	.
48	V20111996	CRT KIT (28") AK52 W/FTZ	PC	1,000	.	.	.	.	.
49	V30002728	28 DEG.COIL&EARTH C.WO/UL FTZ1	PC	1,000	.	.	.	.	.
50	V30016483	CNAS 2P/600 HRZ DIS W/C UL1672AWG24	PC	1,000	.	.	.	.	.
51	V30019083	CNAS 2P/600 SIS W/C+FER UL1007AWG24	PC	1,000	.	.	.	.	.
52	V35000010	EARTH SPRING (4CM)	PC	1,000	.	.	.	.	.
53	V20114688	EXP.KIT AK37 284X-284XW (V.0) TOSHIBA	PC	1,000	.	.	.	.	.
54	V20004520	CABLE HOLDER DX15 (I)	PC	1,000	.	.	.	.	.
55	V60000991	KIRMA - HDPE	KG	0,003	.	.	.	.	.
56	V20084045	STRAP TIE (L:118)	PC	1,000	.	.	.	.	.
57	V60000018	COPOLYMER POLYPROPYLENE	KG	0,001	.	.	.	.	.
58	V20085269	CABLE HOLDER CRT (I) UL94V-0	PC	2,000	.	.	.	.	.
59	V60000855	KIRMA FR-ABS BLUE CRT	KG	0,002	.	.	.	.	.
60	V40006731	ISOLATION COTTON (9x25000mm)	M	1,800	.	.	.	.	.
61	V70000331	ADHESIVE TAPE 75MM/660M (4125)	M	2,592	.	.	.	.	.
62	V20118835	MD.ASY.TK127-XX41-41W 5SW WO/DVD AK52	PC	1,000	.	.	.	.	.
64	V30002181	SWITCH TACT	PC	5,000	SW1	SW2	SW3	SW4	SW5
65	V30019674	LED RED ORANGE 5MM ULTRA BRIGHT	PC	2,000	LD1	LD2	.	.	.
66	V30020822	CNAS 6P/450 FLT W/C+FER UL2468AWG24	PC	1,000	PL1	.	.	.	.
67	V40000084	BRACKET & PREAMPLIFIER	PC	1,000	IC1	.	.	.	.
72	V30000459	RES CF 1/4W 100R J	PC	1,000	R7	.	.	.	.
73	V30000526	RES CF 1/4W 1.5K J	PC	1,000	R2	.	.	.	.
74	V30000622	RES CF 1/4W 270R J	PC	1,000	R5	.	.	.	.
75	V30000689	RES CF 1/4W 3.9K J	PC	1,000	R1	.	.	.	.
76	V30000712	RES CF 1/4W 470R J	PC	1,000	R4	.	.	.	.
77	V30000718	RES CF 1/4W 4.7K J	PC	1,000	R6	.	.	.	.
78	V30000770	RES CF 1/4W 680R J	PC	1,000	R3	.	.	.	.
80	V30022893	PCB 11TK127-6	PC	1,000	.	.	.	.	.
81	V30000371	CAP EL 22UF 50V M	PC	1,000	C1	.	.	.	.
82	V30001455	TR BC558B	PC	1,000	Q1	.	.	.	.
83	V20121334	CRT B.ASSY.TP52E-SING.FOC.(AK52)	PC	1,000	.	.	.	.	.
89	V20121300	CRT B.ASSY.TP52E-PER COMMON AK52	PC	1,000	.	.	.	.	.
90	V35000176	EYELET BR 2*3MM	PC	2,000	PL902	PL903	.	.	.
92	V30000428	SPARK GAP 300V	PC	4,000	SG901	SG902	SG904	SG903	.
93	V30000459	RES CF 1/4W 100R J	PC	2,000	R934	R912	.	.	.
94	V30000466	RES CF 1/4W 1K J	PC	1,000	R911	.	.	.	.
95	V30000477	RES CF 1/4W 100K J	PC	3,000	R905	R906	R909	.	.
96	V30000492	RES CF 1/4W 120R J	PC	1,000	R913	.	.	.	.
97	V30000535	RES CF 1/2W 150K J	PC	1,000	R904	.	.	.	.
98	V30000583	RES CF 1/4W 220R J	PC	3,000	R901	R902	R903	.	.
99	V30000612	RES CF 1/4W 2.4K J	PC	1,000	R914	.	.	.	.
100	V30000788	RES CF 1/4W 6.8M J	PC	1,000	R900	.	.	.	.
101	V30000973	RES MF 1/4W 3.9K F	PC	1,000	R915	.	.	.	.
102	V30001245	RES FUSE 1/4W 0.47R J	PC	1,000	R932	.	.	.	.
103	V30001284	DIODE 1N4148 0.15A/100V 0.5A	PC	2,000	D905	L902-Y	.	.	.
104	V30001318	DIODE BA159 1A/800V 20A	PC	4,000	D902	D901	D903	D904	.
106	V30020603	RES CC 1W 1K K	PC	3,000	R907	R908	R910	.	.
107	V30021483	RES CC 1W 2.2K K	PC	1,000	R933	.	.	.	.
108	V30021532	SPARK GAP 1500V	PC	1,000	SG905	.	.	.	.

BILL OF MATERIAL LIST

10020021 2841 TOSHIBA TOSHIBA 28H37GZ(AK52)

NO	PART NUMBER	DESCRIPTION	UNIT	QTY	POSITION NUMBER				
109	V30021902	PCB 11TP52E	PC	1,000	.	.	.	.	.
110	V30000205	CAP CER 150PF 50V J SL	PC	1,000	C919	.	.	.	.
111	V30000295	CAP CER 100NF 50V Z F	PC	1,000	C917	.	.	.	.
112	V30000330	CAP CER 4.7NF 50V K B	PC	1,000	C904	.	.	.	.
113	V30000352	CAP EL 100UF 16V M	PC	1,000	C918	.	.	.	.
114	V30001427	TR BF422	PC	1,000	Q900	.	.	.	.
115	V30001455	TR BC558B	PC	1,000	Q901	.	.	.	.
118	V30000075	CAP MKT 100NF 250V K (DC)	PC	3,000	C900	C906	C931	.	.
119	V30000350	CAP EL 10UF 250V M	PC	1,000	C905	.	.	.	.
120	V30000415	CAP EL 4.7UF 250V M	PC	1,000	C902	.	.	.	.
122	V30006709	CONN HEADER 5P 2.5MM TOP WHT SD	PC	1,000	PL904	.	.	.	.
123	V30006841	CAP MKP 1.2NF 1.6KV J	PC	1,000	C903	.	.	.	.
124	V30012894	CONN HEADER 10P 2.54MM TOP WHT	PC	1,000	PL905	.	.	.	.
125	V30019071	CABL 1P/550 DIS UL1672AWG22	PC	1,000	PL901	.	.	.	.
126	V35000135	TEST PIN 1.1MM	PC	1,000	PL902	.	.	.	.
128	V20103005	HE.ASY.52-CRT BOARD (AK52)	PC	1,000	IC900	.	.	.	.
129	V30018768	IC TDA6109	PC	1,000	IC900	.	.	.	.
130	V35000131	HEATSINK 11TP18 RGB	PC	1,000	.	.	.	.	.
131	V35000158	NUT C ZN BOTTOM M3	PC	1,000	.	.	.	.	.
132	V35000165	KNURL WASHER C ZNSY 3*6*04 (M3)	PC	1,000	.	.	.	.	.
133	V35000189	SCREW C NI YSMB M3*6	PC	1,000	.	.	.	.	.
134	V30001855	SOCKET CRT NARROWNECK W/GND	PC	1,000	PL900A	.	.	.	.
135	V20124465	CHS.ASSY.52B-139231113212 11G	PC	1,000	.	.	.	.	.
138	V20094516	CHASSIS FRAME AK37 (I) V.0	PC	1,000	.	.	.	.	.
139	V20094517	PCB GUIDE RAIL (HIGH BIG) (I) V.0	PC	2,000	.	.	.	.	.
140	V60000009	FR-HIPS NATR.V-0	KG	0,007	.	.	.	.	.
141	V60000022	MASTERBATCH (BLACK)	G	0,035	.	.	.	.	.
142	V60000009	FR-HIPS NATR.V-0	KG	0,259	.	.	.	.	.
143	V35005061	SCREW RB C SK ZN YFMB 2.9*9.5	PC	4,000	.	.	.	.	.
146	V30001692	FILTER SAW OFWK3953M	PC	1,000	Z950	.	.	.	.
147	V30009833	CABL 1P/100 SIS	PC	1,000	KX22	.	.	.	.
148	V30012545	FILTER SAW K9656M	PC	1,000	Z951	.	.	.	.
150	V30001270	PTC 9 OHM	PC	1,000	TH801	.	.	.	.
151	V30002183	RELAY MON15 KI-S-212M	PC	1,000	RL801	.	.	.	.
153	V30009366	DIODE UF5402 3A/200V 150A	PC	1,000	D811	.	.	.	.
155	V30009637	TUNER WSP (PLL) 38.9 MK2 - BATCH	PC	1,000	TU200	.	.	.	.
157	V30015053	SOCKET SCART NEW TYPE	PC	1,000	PL204	.	.	.	.
159	V20000848	FUSE ASSY.TK79-A (2.5A)	PC	1,000	F801	.	.	.	.
160	V30001731	FUSE 2.5A 250V 5*20MM	PC	1,000	.	.	.	.	.
161	V35000136	FUSE HOLDER TK79-A (GRAY)	PC	1,000	.	.	.	.	.
163	V20070614	HE.ASY.37-SMPS 170-270V	PC	1,000	Q802	.	.	.	.
164	V30001386	TR MTP6N60E (PLASTIC)	PC	1,000	.	.	.	.	.
165	V35000158	NUT C ZN BOTTOM M3	PC	1,000	.	.	.	.	.
166	V35000165	KNURL WASHER C ZNSY 3*6*04 (M3)	PC	1,000	.	.	.	.	.
167	V35000181	SCREW C ZN YSMB M3*8	PC	1,000	.	.	.	.	.
168	V35006413	HEATSINK SMPS AK45	PC	1,000	.	.	.	.	.
169	V70000074	SILICON (GRES)	KG	0,010	.	.	.	.	.
170	V20085393	HE.ASY.33-DIODE UF5407 (33/52)	PC	1,000	D805	.	.	.	.
171	V30001964	FERRITE BAR 5*8	PC	1,000	.	.	.	.	.
172	V30007681	DIODE UF5407 3A/800V 150A	PC	1,000	.	.	.	.	.
173	V35004134	HEATSINK DIODE (2)	PC	1,000	.	.	.	.	.
174	V20102765	HE.ASY.52A-SMPS REG2	PC	1,000	.	.	.	.	.
175	V30001500	IC LM7808	PC	1,000	IC803	.	.	.	.
176	V35000142	HEATSINK 15AK14/15 15/TP ORTAK	PC	1,000	.	.	.	.	.
177	V35000158	NUT C ZN BOTTOM M3	PC	1,000	.	.	.	.	.
178	V35000165	KNURL WASHER C ZNSY 3*6*04 (M3)	PC	1,000	.	.	.	.	.
179	V35000180	SCREW C ZN YSMB M3*6	PC	1,000	.	.	.	.	.
180	V20102766	HE.ASY.52A-VERTICAL	PC	1,000	.	.	.	.	.
181	V30007799	TR BDX53BFI	PC	1,000	Q104	.	.	.	.
182	V30013687	IC TDA8177F	PC	1,000	IC100	.	.	.	.
183	V35000158	NUT C ZN BOTTOM M3	PC	2,000	.	.	.	.	.
184	V35000166	KNURL WASHER C NI 3.2*6.5*0.6	PC	2,000	.	.	.	.	.
185	V35000181	SCREW C ZN YSMB M3*8	PC	2,000	.	.	.	.	.
186	V35005353	HEATSINK VERTICAL AK52	PC	1,000	.	.	.	.	.
187	V70000074	SILICON (GRES)	G	0,010	.	.	.	.	.
188	V20102767	HE.ASY.52A-HORIZANTAL	PC	1,000	.	.	.	.	.
189	V30007678	DIODE GUC DTV32F1500A 6A/1500V 100A	PC	1,000	D104	.	.	.	.
190	V30007768	DIODE STTA506F 5A/600V 55A	PC	1,000	D105	.	.	.	.
191	V30016686	TR 2SC5302	PC	1,000	Q101	.	.	.	.
192	V35000158	NUT C ZN BOTTOM M3	PC	3,000	.	.	.	.	.
193	V35000166	KNURL WASHER C NI 3.2*6.5*0.6	PC	3,000	.	.	.	.	.
194	V35000181	SCREW C ZN YSMB M3*8	PC	2,000	.	.	.	.	.
195	V35000182	SCREW C ZN YSMB M3*10	PC	1,000	.	.	.	.	.
196	V35005354	HEATSINK HORIZONTAL AK52	PC	1,000	.	.	.	.	.
197	V20106073	HE.ASY.17PW02-STEPDOWN	PC	1,000	Q813	.	.	.	.
198	V30007802	TR STP20N06LFP	PC	1,000	.	.	.	.	.
199	V35000142	HEATSINK 15AK14/15 15/TP ORTAK	PC	1,000	.	.	.	.	.
200	V35000158	NUT C ZN BOTTOM M3	PC	1,000	.	.	.	.	.
201	V35000165	KNURL WASHER C ZNSY 3*6*04 (M3)	PC	1,000	.	.	.	.	.
202	V35000183	SCREW C ZN YSMB M3*12	PC	1,000	.	.	.	.	.
203	V20108354	DIODE BRIDGE GBU4M 4A/1000V 150A(FORMLU)	PC	1,000	D810	.	.	.	.
204	V30007758	DIODE BRIDGE GBU4M 4A/1000V 150A	PC	1,000	.	.	.	.	.
205	V20108636	HE.ASY.52A-LM1086 3.3 1.5A 15AK14/15 ORT	PC	1,000	.	.	.	.	.
206	V30019617	IC LDO LM1086 3.3V/1.5A TO220	PC	1,000	IC812	.	.	.	.
207	V35000142	HEATSINK 15AK14/15 15/TP ORTAK	PC	1,000	.	.	.	.	.
208	V35000158	NUT C ZN BOTTOM M3	PC	1,000	.	.	.	.	.
209	V35000165	KNURL WASHER C ZNSY 3*6*04 (M3)	PC	1,000	.	.	.	.	.
210	V35000183	SCREW C ZN YSMB M3*12	PC	1,000	.	.	.	.	.
211	V30000094	CAP MKT 220NF 275V M AC	PC	1,000	C801	.	.	.	.
212	V30000161	CAP MKP 47NF 630V J	PC	1,000	C805	.	.	.	.
213	V30000350	CAP EL 10UF 250V M	PC	1,000	C117	.	.	.	.
214	V30000360	CAP EL 1000UF 25V M	PC	6,000	C120	C124	C826	C825	C851
.	.	.	.	.	C842	.	.	.	.
215	V30000383	CAP EL 2200UF 25V M	PC	4,000	C821	C822	C424	C432	.
216	V30000402	CAP EL 47UF 100V M	PC	1,000	C119	.	.	.	.

BILL OF MATERIAL LIST

10020021 2841 TOSHIBA TOSHIBA 28H37GZ(AK52)

NO	PART NUMBER	DESCRIPTION	UNIT	QTY	POSITION NUMBER				
217	V30000411	CAP EL 4700UF 16V M	PC	1,000	C834	.	.	.	.
218	V30000415	CAP EL 4.7UF 250V M	PC	1,000	C113	.	.	.	.
219	V30000421	CAP EL 220UF 400V M (FOR 28")	PC	1,000	C807	.	.	.	.
220	V30000440	CAP CER 2.2NF 4KV M	PC	2,000	C810	C850	.	.	.
222	V30001077	RES MO 2W 10R J	PC	2,000	R145	R180	.	.	.
223	V30001079	RES MO 1W 100R J	PC	1,000	R104	.	.	.	.
224	V30001086	RES MO 2W 10K J	PC	1,000	R116	.	.	.	.
225	V30001168	RES MO 2W 470RJ	PC	1,000	R117	.	.	.	.
226	V30001174	RES MO 2W 0.47R J	PC	2,000	R833	R828	.	.	.
227	V30001224	RES FUSE 1/2W 0.22R J	PC	1,000	R844	.	.	.	.
228	V30001288	DIODE BYV27-200 2A/200V 50A	PC	1,000	D808	.	.	.	.
229	V30001299	DIODE UF5404 3A/400V 150A	PC	2,000	D108	D109	.	.	.
230	V30001762	CONN HEADER 2P 2.5MM(9.7MM) TOP	PC	1,000	PL405	.	.	.	.
231	V30001764	CONN HEADER 2P 2.5MM(9.7MM) TOP BLACK	PC	1,000	PL406	.	.	.	.
232	V30001783	CONN HEADER 5P 2.5MM TOP BD	PC	1,000	PL408	.	.	.	.
233	V30001792	CONN HEADER 2P 7.5MM TOP WHT	PC	2,000	PL103	PL802	.	.	.
234	V30001795	CONN HEADER 3P 5/7.5MM TOP WHT	PC	1,000	PL801	.	.	.	.
235	V30001829	CONN HEADER 2P 2.5MM TOP WHT SD	PC	1,000	PL105	.	.	.	.
236	V30001960	FERIT BAR 6*20MM AK16	PC	2,000	L419	L420	.	.	.
237	V30002851	XTAL 4MHZ L.C=30PF	PC	1,000	X951	.	.	.	.
238	V30006709	CONN HEADER 5P 2.5MM TOP WHT SD	PC	1,000	PL101	.	.	.	.
239	V30006743	TRF. HORIZONTAL DRIVER 15AK17-17"	PC	1,000	TR100	.	.	.	.
240	V30006909	CAP EL 100UF M 250V	PC	2,000	C816	C115	.	.	.
241	V30007757	COIL INJECTION EW 6MH AK28	PC	1,000	L101	.	.	.	.
242	V30007771	FIXED COIL 100UH	PC	1,000	L100	.	.	.	.
243	V30009366	DIODE UF5402 3A/200V 150A	PC	3,000	D803	D804	D824	.	.
244	V30009846	CABL 1P/40 SIS	PC	2,000	PL418-PL4	PL420-PL4	.	.	.
246	V30010921	DOUBLE-DECK SCART SOCKET	PC	1,000	PL203	.	.	.	.
248	V30011968	IC SMPS MC44608 DIP8	PC	1,000	IC804	.	.	.	.
249	V30015087	IC OPTOCOUPLER TCET1102G	PC	1,000	IC801	.	.	.	.
250	V30017799	CNAS 5P/500 TUB SIS W/DC UL1007AWG24	PC	1,000	PL101	.	.	.	.
251	V30018078	LINE FILTER 2X22MH (AK37)	PC	1,000	L805	.	.	.	.
252	V30018412	CONN HOUSING 35P 3.0MM TOP DR	PC	2,000	PL409	PL410	.	.	.
253	V30018422	IC AAMP TDA7480L 10W PDIP20	PC	2,000	IC401	IC402	.	.	.
255	V30018627	TR NMOS IRFU110 4.3A/100V TO251	PC	1,000	Q100	.	.	.	.
256	V30019205	TRF SMPS AK52 (170-270V) 170W	PC	1,000	TR801	.	.	.	.
258	V30020772	CNAS 10P/320 AK52 SHL W/DC UL1533AWG24	PC	1,000	PL853	.	.	.	.
259	V30020805	CABL 1P/150 SIS W/FER	PC	1,000	KXX1	.	.	.	.
260	V40011350	SPACER SUPPORT SCC-3C-NZW	PC	1,000	.	.	.	.	.
261	V40011922	EDGE SADDLE (CT-16)	PC	2,000	.	.	.	.	.
262	V70000029	SOLDER (INGOT) 63/37	KG	0,020	.	.	.	.	.
263	V70000661	SILICON V0 (UL 1410)(Firma Catg.No3748	G	5,000	.	.	.	.	.
265	V30000075	CAP MKT 100NF 250V K (DC)	PC	1,000	C861	.	.	.	.
266	V30001792	CONN HEADER 2P 7.5MM TOP WHT	PC	1,000	PL804	.	.	.	.
267	V30018085	CAP VAR 510V K MFCN14D511	PC	1,000	R870	.	.	.	.
274	V30001457	TR BC848B SMD	PC	1,000	Q950	.	.	.	.
275	V30012411	DIODE BA782 SMD	PC	1,000	D961	.	.	.	.
276	V30012603	CAP SMD 100NF 25V K R (0603)	PC	1,000	C958	.	.	.	.
277	V30012657	RES SMD 1/16W 1K J (0603)	PC	1,000	R963	.	.	.	.
278	V30012659	RES SMD 1/16W 2.2K J (0603)	PC	1,000	R962	.	.	.	.
279	V30012685	RES SMD 1/16W 33K J (0603)	PC	1,000	R960	.	.	.	.
280	V30012705	RES SMD 1/16W 6.8K J (0603)	PC	1,000	R961	.	.	.	.
282	V30016126	CAP SMD 220NF 16V K R (0603)	PC	1,000	C996	.	.	.	.
283	V30021083	IC TDA9886T/V3-SO24	PC	1,000	IC954	.	.	.	.
288	V30000466	RES CF 1/4W 1K J	PC	1,000	R843	.	.	.	.
289	V30000352	CAP EL 100UF 16V M	PC	1,000	C840	.	.	.	.
290	V30001454	TR BC548B	PC	1,000	Q801	.	.	.	.
291	V30001285	DIODE 1N4148 SMD	PC	1,000	D830	.	.	.	.
292	V30001457	TR BC848B SMD	PC	1,000	Q808	.	.	.	.
293	V30012641	RES SMD 1/16W 10K J (0603)	PC	2,000	R808	R842	.	.	.
294	V30012692	RES SMD 1/16W 4.7K J (0603)	PC	1,000	R807	.	.	.	.
296	V30009699	DIODE ZENER SMD BZT55C12	PC	1,000	D207	.	.	.	.
297	V30012581	CAP SMD 1NF 50V K R (0603)	PC	2,000	C274	C284	.	.	.
298	V30012589	CAP SMD 4.7NF 50V K (0603)	PC	2,000	C276	C287	.	.	.
299	V30012592	CAP SMD 6.8NF 50V K (0603)	PC	2,000	C270	C271	.	.	.
300	V30012607	CAP SMD 150PF 50V J (0603)	PC	4,000	C273	C280	C289	C290	.
301	V30012707	RES SMD 1/16W 680R J (0603)	PC	2,000	R230	R235	.	.	.
302	V30013413	FERRITE BEAD ACB2012H-300	PC	4,000	L224	L225	L226	L228	.
303	V30018735	DIODE ZENER BZT55C15 15V SMD	PC	1,000	D206	.	.	.	.
312	V30000918	RES MF 1/4W 2.1K F	PC	1,000	R121	.	.	.	.
313	V30001036	RES MF 1/4W 95K F	PC	1,000	R123	.	.	.	.
314	V30001131	RES MO 1W 0.22R J	PC	1,000	R103	.	.	.	.
315	V30001291	DIODE HER107 1A/800V 30A	PC	1,000	D100	.	.	.	.
316	V30007783	RES FUSE 1/4W 2.2R J	PC	1,000	R122	.	.	.	.
317	V30000078	CAP MKT 1UF 100V M	PC	1,000	C129	.	.	.	.
318	V30000319	CAP CER 2.7NF 500V K B	PC	1,000	C808	.	.	.	.
319	V30001435	TR NBJT BC639 1A/100V TO92	PC	1,000	Q809	.	.	.	.
320	V30012509	RES SMD 1/16W 100K J (0603)	PC	1,000	R113	.	.	.	.
321	V30012567	CAP SMD 220PF 50V J (0603)	PC	1,000	C108	.	.	.	.
330	V30000452	RES CF 1/4W 10R J	PC	1,000	R806	.	.	.	.
331	V30000459	RES CF 1/4W 100R J	PC	3,000	R952	R954	R995	.	.
332	V30000466	RES CF 1/4W 1K J	PC	2,000	R118	R832	.	.	.
333	V30000477	RES CF 1/4W 100K J	PC	3,000	R829	R136	R157	.	.
334	V30000481	RES CF 1/4W 1M J	PC	1,000	R804	.	.	.	.
335	V30000515	RES CF 1/4W 15R J	PC	1,000	R429	.	.	.	.
336	V30000531	RES CF 1/4W 15K J	PC	1,000	R186	.	.	.	.
337	V30000541	RES CF 1/4W 1.5M J	PC	1,000	R146	.	.	.	.
338	V30000564	RES CF 1/4W 18K J	PC	1,000	R126	.	.	.	.
339	V30000583	RES CF 1/4W 220R J	PC	1,000	R105	.	.	.	.
340	V30000622	RES CF 1/4W 270R J	PC	1,000	R165	.	.	.	.
341	V30000628	RES CF 1/4W 2.7K J	PC	1,000	R169	.	.	.	.
342	V30000660	RES CF 1/4W 3.3K J	PC	1,000	R866	.	.	.	.
343	V30000718	RES CF 1/4W 4.7K J	PC	6,000	R110	R127	R823	R824	R860
.	.	.	.	.	R802	.	.	.	.
344	V30000729	RES CF 1/4W 470K J	PC	1,000	R129	.	.	.	.

BILL OF MATERIAL LIST

10020021 2841 TOSHIBA TOSHIBA 28H37GZ(AK52)

NO	PART NUMBER	DESCRIPTION	UNIT	QTY	POSITION NUMBER				
345	V30000744	RES CF 1/4W 560R J	PC	1,000	R147	.	.	.	.
346	V30000769	RES CF 1/2W 680R J	PC	2,000	R820	R821	.	.	.
347	V30000784	RES CF 1/4W 680K J	PC	1,000	R155	.	.	.	.
348	V30000792	RES CF 1/4W 75R J	PC	1,000	R998	.	.	.	.
349	V30000918	RES MF 1/4W 2.1K F	PC	1,000	R856	.	.	.	.
350	V30000925	RES MF 1/4W 2.2K F	PC	1,000	R855	.	.	.	.
351	V30000983	RES MF 1/4W 4.7K F	PC	1,000	R805	.	.	.	.
352	V30001011	RES MF 1/4W 6.8K F	PC	2,000	R142	R143	.	.	.
353	V30001036	RES MF 1/4W 95K F	PC	1,000	R156	.	.	.	.
354	V30001159	RES MO 1W 0.33R J	PC	1,000	R810	.	.	.	.
355	V30001257	RES MG 1/2W 4.7M J	PC	1,000	R812	.	.	.	.
356	V30001284	DIODE 1N4148 0.15A/100V 0.5A	PC	2,000	D826	D404	.	.	.
357	V30001288	DIODE BYV27-200 2A/200V 50A	PC	1,000	D111	.	.	.	.
358	V30001291	DIODE HER107 1A/800V 30A	PC	3,000	D106	D107	D110	.	.
359	V30001318	DIODE BA159 1A/800V 20A	PC	7,000	D120	D801	D814	D815	D829
.	.	.	.	.	D818	D123	.	.	.
360	V30001323	DIODE BY299 2A/800V 70A	PC	1,000	D802	.	.	.	.
361	V30001329	DIODE 1N4007 1A/1000V 30A	PC	2,000	D812	D831	.	.	.
362	V30001344	DIODE ZENER 6.2V 1/2W	PC	1,000	D806	.	.	.	.
363	V30001377	DIODE ZENER 33V UZT 33B	PC	1,000	D113	.	.	.	.
364	V30001979	FIXED COIL 1UH Q45 M-A	PC	1,000	L951	.	.	.	.
365	V30001992	FIXED COIL 10UH Q65 K-A	PC	1,000	L803	.	.	.	.
366	V30001996	FIXED COIL 22UH Q40 K	PC	1,000	L109	.	.	.	.
367	V30006691	DIODE ZENER 3.3V	PC	1,000	D813	.	.	.	.
368	V30006712	FERRITE BEAD 3.5X4.7X0.8	PC	5,000	L105	L106	L417	L418	J130
369	V30009036	RES FUSE 1/2W 0.1R J	PC	1,000	R125	.	.	.	.
370	V30025350	PCB 11AK52B6	PC	1,000	.	.	.	.	.
371	V30000069	CAP MKT 1NF 100V J	PC	4,000	C469	C470	C472	C473	.
372	V30000071	CAP MKT 10NF 63V J	PC	2,000	C405	C466	.	.	.
373	V30000074	CAP MKT 100NF 63V J	PC	1,000	C142	.	.	.	.
374	V30000099	CAP MKT 33NF 63V J	PC	1,000	C812	.	.	.	.
375	V30000100	CAP MKT 330NF 63V J	PC	4,000	C408	C428	C411	C431	.
376	V30000109	CAP MKT 470NF 63V J	PC	2,000	C963	C966	.	.	.
377	V30000190	CAP CER 100PF 50V J CH	PC	1,000	C864	.	.	.	.
378	V30000283	CAP CER 1NF 50V K B	PC	1,000	C131	.	.	.	.
379	V30000286	CAP CER 1NF 500V K B	PC	1,000	C145	.	.	.	.
380	V30000295	CAP CER 100NF 50V Z F	PC	6,000	C831	C430	C824	C410	C409
.	.	.	.	.	C429	.	.	.	.
381	V30000296	CAP CER 100NF 100V Z F	PC	3,000	C146	C128	C148	.	.
382	V30000302	CAP CER 1.8NF 50V KB	PC	2,000	C123	C130	.	.	.
383	V30000345	CAP EL 10UF 50V M	PC	5,000	C104	C210	C953	C954	C970
384	V30000346	CAP EL 10UF 100V M	PC	1,000	C107	.	.	.	.
385	V30000352	CAP EL 100UF 16V M	PC	2,000	C856	C468	.	.	.
386	V30000353	CAP EL 100UF 25V M	PC	5,000	C101	C462	C463	C464	C465
387	V30000362	CAP EL 1UF 50V M	PC	1,000	C106	.	.	.	.
388	V30000367	CAP EL 1UF 250V M	PC	2,000	C837	C862	.	.	.
389	V30000375	CAP EL 220UF 16V M	PC	1,000	C857	.	.	.	.
390	V30000387	CAP EL 33UF 50V M	PC	1,000	C804	.	.	.	.
391	V30000393	CAP EL 3.3UF 50V M	PC	2,000	C845	C134	.	.	.
392	V30000400	CAP EL 47UF 50V M	PC	3,000	C139	C828	C956	.	.
393	V30000431	CAP CER 100PF 1KV M	PC	1,000	C116	.	.	.	.
394	V30000433	CAP CER 1NF 1KV M B	PC	3,000	C843	C471	C474	.	.
395	V30001384	TR MCR22-6	PC	1,000	Q817	.	.	.	.
396	V30001428	TR BF423	PC	1,000	Q806	.	.	.	.
397	V30001454	TR BC548B	PC	4,000	Q105	Q803	Q805	Q810	.
398	V30001455	TR BC558B	PC	1,000	Q814	.	.	.	.
399	V30001506	IC TL431	PC	3,000	Q116	Q815	Q816	.	.
400	V30007308	CAP CER 220PF 1KV K (PULSE)	PC	4,000	C806	C813	C814	C815	.
401	V30009208	CAP CER 470PF 1KV K (PULSE)	PC	1,000	C809	.	.	.	.
402	V30019641	CAP MKT 100NF 100V J NO-HIT	PC	1,000	C135	.	.	.	.
403	V30000284	CAP SMD 1NF 50V K R (0805)	PC	1,000	C301	.	.	.	.
404	V30000294	CAP SMD 100NF 50V K (0805)	PC	10,000	C100	C125	C126	C803	C823
.	.	.	.	.	C827	C846	C859	C817	C818
405	V30000309	CAP SMD 2.2NF 50V K R 0805	PC	1,000	C811	.	.	.	.
406	V30000469	RES SMD 1/10W 1K J 0805	PC	2,000	R827	R834	.	.	.
407	V30000475	RES SMD 1/10W 10K J 0805	PC	4,000	R148	R161	R830	R835	.
408	V30000503	RES SMD 1/10W 12K J (0805)	PC	1,000	R837	.	.	.	.
409	V30000517	RES SMD 1/10W 15R J 0805	PC	1,000	R838	.	.	.	.
410	V30000529	RES SMD 1/10W 1.5K J	PC	2,000	R102	R166	.	.	.
411	V30000593	RES SMD 1/10W 2.2K J (0805)	PC	3,000	R803	R836	R108	.	.
412	V30000614	RES SMD 1/10W 2.4K J (0805)	PC	1,000	R814	.	.	.	.
413	V30000626	RES SMD 1/10W 270R J	PC	1,000	R171	.	.	.	.
414	V30000631	RES SMD 1/10W 2.7K J 0805	PC	1,000	R131	.	.	.	.
415	V30000636	RES SMD 1/10W 27K J 0805	PC	1,000	R138	.	.	.	.
416	V30000710	RES SMD 1/10W 47R J (0805)	PC	1,000	R813	.	.	.	.
417	V30000721	RES SMD 1/10W 4.7K J	PC	3,000	R159	R162	R160	.	.
418	V30000782	RES SMD 1/10W 68K J	PC	2,000	R818	R868	.	.	.
419	V30001285	DIODE 1N4148 SMD	PC	15,000	D114	D117	D118	D119	D807
.	.	.	.	.	D809	D820	D821	D819	D823
.	.	.	.	.	D127	D128	D951	D962	D963
420	V30001457	TR BC848B SMD	PC	9,000	Q112	Q113	Q114	Q200	Q804
.	.	.	.	.	Q807	Q108	Q811	Q952	.
421	V30001458	TR BC858B SMD	PC	7,000	Q102	Q103	Q106	Q115	Q812
.	.	.	.	.	Q400	Q117	.	.	.
424	V30001971	FERRITE BEAT (805) BLM21A601S	PC	1,000	L802	.	.	.	.
425	V30007026	RES SMD 1/10W 5.1K J(0805)	PC	1,000	R831	.	.	.	.
426	V30007760	DIODE ZENER SMD BZT55C10	PC	1,000	D102	.	.	.	.
427	V30007763	DIODE ZENER SMD BZT55C5V1	PC	4,000	D103	D112	D201	D827	.
428	V30007789	RES SMD 1/10W 27K F (0805)	PC	1,000	R137	.	.	.	.
429	V30009699	DIODE ZENER SMD BZT55C12	PC	4,000	D822	D202	D203	D124	.
430	V30010560	CAP SMD 220NF 25V K R (0805)	PC	1,000	R163	.	.	.	.
431	V30010643	RES SMD 1/10W 39R J (0805)	PC	1,000	R970	.	.	.	.
432	V30012506	RES SMD 1/16W 1.5K J (0603)	PC	1,000	R187	.	.	.	.
433	V30012508	RES SMD 1/16W 1.8K J (0603)	PC	1,000	R406	.	.	.	.
434	V30012510	RES SMD 1/16W 100R J (0603)	PC	4,000	R815	R953	R955	R964	.

BILL OF MATERIAL LIST

10020021 2841 TOSHIBA TOSHIBA 28H37GZ(AK52)

NO	PART NUMBER	DESCRIPTION	UNIT	QTY	POSITION NUMBER				
435	V30012560	CAP SMD 100PF 50V J (0603)	PC	2,000	C467	C950	.	.	.
436	V30012566	CAP SMD 22PF 50V J (0603)	PC	1,000	C965	.	.	.	.
437	V30012567	CAP SMD 220PF 50V J (0603)	PC	1,000	C852	.	.	.	.
438	V30012568	CAP SMD 270PF 50V J (0603)	PC	2,000	C406	C426	.	.	.
439	V30012569	CAP SMD 33PF 50V J (0603)	PC	4,000	C952	C955	C959	C960	.
440	V30012572	CAP SMD 390PF 50V J (0603)	PC	1,000	C962	.	.	.	.
441	V30012574	CAP SMD 470PF 50V J (0603)	PC	1,000	C867	.	.	.	.
442	V30012581	CAP SMD 1NF 50V K R (0603)	PC	7,000	C240	C249	C839	C140	C994
.	.	.	.	.	C1006	C1007	.	.	.
443	V30012582	CAP SMD 10NF 50V K R (0603)	PC	2,000	C961	C969	.	.	.
444	V30012583	CAP SMD 1.5NF 50V K (0603)	PC	1,000	C968	.	.	.	.
445	V30012585	CAP SMD 2.2NF 50V K R (0603)	PC	2,000	C407	C427	.	.	.
446	V30012589	CAP SMD 4.7NF 50V K (0603)	PC	8,000	C243	C244	C245	C247	C250
.	.	.	.	.	C251	C419	C433	.	.
447	V30012590	CAP SMD 47NF 50V K (0603)	PC	1,000	C105	.	.	.	.
448	V30012592	CAP SMD 6.8NF 50V K (0603)	PC	1,000	C237	.	.	.	.
449	V30012592	CAP SMD 6.8NF 50V K (0603)	PC	3,000	C233	C235	C236	.	.
450	V30012603	CAP SMD 100NF 25V K R (0603)	PC	9,000	C420	C458	C423	C455	C456
.	.	.	.	.	C421	C853	C951	C972	.
451	V30012607	CAP SMD 150PF 50V J (0603)	PC	16,000	C239	C241	C246	C248	C252
.	.	.	.	.	C253	C256	C261	C262	C263
.	.	.	.	.	C266	C267	C307	C308	C309
.	.	.	.	.	C310	.	.	.	.
452	V30012610	CAP SMD 10NF 50V J (0603)	PC	1,000	C964	.	.	.	.
453	V30012641	RES SMD 1/16W 10K J (0603)	PC	11,000	R119	R822	R825	R839	R840
.	.	.	.	.	R849	R158	R853	R861	R862
.	.	.	.	.	R819	.	.	.	.
454	V30012644	RES SMD 1/16W 12K J (0603)	PC	1,000	R966	.	.	.	.
455	V30012657	RES SMD 1/16W 1K J (0603)	PC	7,000	R207	R841	R859	R854	R424
.	.	.	.	.	R863	S802	.	.	.
456	V30012659	RES SMD 1/16W 2.2K J (0603)	PC	10,000	R107	R109	R112	R115	R847
.	.	.	.	.	R848	R851	R852	R850	R951
457	V30012662	RES SMD 1/16W 2.7K J (0603)	PC	1,000	R111	.	.	.	.
458	V30012668	RES SMD 1/16W 220R J (0603)	PC	1,000	R994	.	.	.	.
459	V30012669	RES SMD 1/16W 22K J (0603)	PC	2,000	R972	R973	.	.	.
460	V30012677	RES SMD 1/16W 3.3K J (0603)	PC	1,000	R422	.	.	.	.
461	V30012682	RES SMD 1/16W 30K J (0603)	PC	1,000	R403	.	.	.	.
462	V30012684	RES SMD 1/16W 330R J (0603)	PC	1,000	R968	.	.	.	.
463	V30012689	RES SMD 1/16W 39K J (0603)	PC	1,000	R867	.	.	.	.
464	V30012692	RES SMD 1/16W 4.7K J (0603)	PC	2,000	R106	R185	.	.	.
465	V30012695	RES SMD 1/16W 470R J (0603)	PC	3,000	R845	R864	R993	.	.
466	V30012696	RES SMD 1/16W 47K J (0603)	PC	2,000	R120	R967	.	.	.
467	V30012698	RES SMD 1/16W 5.6K J (0603)	PC	1,000	R418	.	.	.	.
468	V30012698	RES SMD 1/16W 5.6K J (0603)	PC	1,000	R958	.	.	.	.
469	V30012705	RES SMD 1/16W 6.8K J (0603)	PC	2,000	R922	R965	.	.	.
470	V30012707	RES SMD 1/16W 680R J (0603)	PC	4,000	R215	R216	R217	R218	.
471	V30012712	RES SMD 1/16W 8.2K J (0603)	PC	3,000	R132	R409	R417	.	.
472	V30012714	RES SMD 1/16W 820R J (0603)	PC	1,000	R1006	.	.	.	.
473	V30012982	RES SMD 1/16W 10R J 0603	PC	2,000	S408	S409	.	.	.
475	V30013413	FERRITE BEAD ACB2012H-300	PC	8,000	L213	L214	L215	L216	L217
.	.	.	.	.	L218	L219	L220	.	.
476	V30013413	FERRITE BEAD ACB2012H-300	PC	1,000	L999	.	.	.	.
477	V30014022	RES SMD 1/16W 47R J (0603)	PC	2,000	R205	R997	.	.	.
478	V30014420	RES SMD 1/16W 10K F (0603)	PC	1,000	R415	.	.	.	.
479	V30016126	CAP SMD 220NF 16V K R (0603)	PC	1,000	C967	.	.	.	.
480	V30016654	CAP SMD 100NF 16V K R (0603)	PC	3,000	C848	C212	C858	.	.
481	V30018735	DIODE ZENER BZT55C15 15V SMD	PC	2,000	D204	D205	.	.	.
482	V20124423	MD.ASY.FB52A-311112111321211	PC	1,000	.	.	.	.	.
484	V20101701	MD.SMD.FB52A-FAV IN	PC	1,000	.	.	.	.	.
486	V30000074	CAP MKT 100NF 63V J	PC	1,000	C882	.	.	.	.
487	V30000315	CAP SMD 220NF 25V Z (0805)	PC	2,000	C408	C409	.	.	.
488	V30001971	FERRITE BEAT (805) BLM21A601S	PC	1,000	L850	.	.	.	.
489	V30012581	CAP SMD 1NF 50V K R (0603)	PC	2,000	C415	C416	.	.	.
490	V30012589	CAP SMD 4.7NF 50V K (0603)	PC	2,000	C473	C474	.	.	.
491	V30012657	RES SMD 1/16W 1K J (0603)	PC	2,000	R437	R438	.	.	.
492	V30012713	RES SMD 1/16W 75R J (0603)	PC	1,000	R891	.	.	.	.
493	V30017143	COIL SMD 22UH (2520)	PC	2,000	L407	L408	.	.	.
494	V20101763	MD.SMD.FB52A-HEADPHONE	PC	1,000	.	.	.	.	.
496	V30000345	CAP EL 10UF 50V M	PC	1,000	C481	.	.	.	.
497	V30000352	CAP EL 100UF 16V M	PC	2,000	C430	C432	.	.	.
498	V30000362	CAP EL 1UF 50V M	PC	1,000	C433	.	.	.	.
499	V30000315	CAP SMD 220NF 25V Z (0805)	PC	2,000	C426	C427	.	.	.
500	V30001285	DIODE 1N4148 SMD	PC	2,000	D404	D405	.	.	.
501	V30001971	FERRITE BEAT (805) BLM21A601S	PC	2,000	L400	L401	.	.	.
502	V30010024	IC TDA1308T SOIC 8P	PC	1,000	IC401	.	.	.	.
503	V30012567	CAP SMD 220PF 50V J (0603)	PC	2,000	C477	C478	.	.	.
504	V30012581	CAP SMD 1NF 50V K R (0603)	PC	2,000	C431	C435	.	.	.
505	V30012589	CAP SMD 4.7NF 50V K (0603)	PC	4,000	C443	C444	C429	C434	.
506	V30012592	CAP SMD 6.8NF 50V K (0603)	PC	2,000	C401	C403	.	.	.
507	V30012641	RES SMD 1/16W 10K J (0603)	PC	2,000	R412	R416	.	.	.
508	V30012692	RES SMD 1/16W 4.7K J (0603)	PC	2,000	R411	R413	.	.	.
509	V30012700	RES SMD 1/16W 51K J (0603)	PC	2,000	R414	R415	.	.	.
511	V30016654	CAP SMD 100NF 16V K R (0603)	PC	1,000	C428	.	.	.	.
512	V30017143	COIL SMD 22UH (2520)	PC	2,000	L409	L410	.	.	.
513	V20101768	MD.SMD.FB52A-WO/PIP	PC	1,000	.	.	.	.	.
515	V20101771	MD.SMD.FB52A-VIRTUAL DOLBY&3D PANORAMA	PC	1,000	.	.	.	.	.
516	V30018653	IC MSP3411G PLQFP64	PC	1,000	IC400	.	.	.	.
517	V20105455	MD.SMD.FB52A-WO/DVD	PC	1,000	.	.	.	.	.
519	V20126358	MD.SMD.FB52A3-COMMON(TOSHIBA)	PC	1,000	.	.	.	.	.
522	V30023510	PCB 11FB52A4	PC	1,000	.	.	.	.	.
523	V30000068	CAP MKT 1NF 63V K	PC	1,000	C604	.	.	.	.
524	V30000074	CAP MKT 100NF 63V J	PC	4,000	C878	C879	C881	C912	.
525	V30000109	CAP MKT 470NF 63V J	PC	3,000	C642	C643	C688	.	.
526	V30000345	CAP EL 10UF 50V M	PC	17,000	C638	C639	C640	C641	C644
.	.	.	.	.	C645	C659	C660	C665	C689

BILL OF MATERIAL LIST

10020021 2841 TOSHIBA TOSHIBA 28H37GZ(AK52)

NO	PART NUMBER	DESCRIPTION	UNIT	QTY	POSITION NUMBER				
.	.	.	.	.	C690	C748	C413	C414	C448
.	.	.	.	.	C450	C697	.	.	.
527	V30000352	CAP EL 100UF 16V M	PC	4,000	C722	C723	C873	C402	.
528	V30000362	CAP EL 1UF 50V M	PC	1,000	C731	.	.	.	.
529	V30000362	CAP EL 1UF 50V M	PC	2,000	C735	C755	.	.	.
530	V30000371	CAP EL 22UF 50V M	PC	11,000	C671	C674	C726	C729	C738
.	.	.	.	.	C437	C439	C436	C438	C479
.	.	.	.	.	C480	.	.	.	.
531	V30000393	CAP EL 3.3UF 50V M	PC	2,000	C663	C412	.	.	.
532	V30000396	CAP EL 47UF 16V M	PC	1,000	C754	.	.	.	.
533	V30000413	CAP EL 4.7UF 50V M	PC	1,000	C753	.	.	.	.
534	V30000444	CAP CER 470PF 1KV KB	PC	1,000	C472	.	.	.	.
535	V30000315	CAP SMD 220NF 25V Z (0805)	PC	15,000	C406	C407	C451	C452	C680
.	.	.	.	.	C683	C694	C907	C908	C909
.	.	.	.	.	C453	C454	C888	C890	C892
536	V30001285	DIODE 1N4148 SMD	PC	8,000	D401	D402	D403	D600	D601
.	.	.	.	.	D602	D604	D750	.	.
537	V30001457	TR BC848B SMD	PC	36,000	Q401	Q402	Q600	Q601	Q602
.	.	.	.	.	Q603	Q605	Q606	Q610	Q612
.	.	.	.	.	Q613	Q614	Q721	Q722	Q723
.	.	.	.	.	Q724	Q725	Q726	Q727	Q729
.	.	.	.	.	Q730	Q850	Q856	Q859	Q861
.	.	.	.	.	Q863	Q731	Q732	Q733	Q403
.	.	.	.	.	Q404	Q852	Q720	Q750	Q751
.	.	.	.	.	Q752	.	.	.	.
538	V30001458	TR BC858B SMD	PC	7,000	Q400	Q607	Q608	Q609	Q611
.	.	.	.	.	Q728	Q734	.	.	.
539	V30001971	FERRITE BEAT (805) BLM21A601S	PC	5,000	L406	L411	L418	L602	L861
540	V30003720	DIODE ZENER BZT55C5V6 5.6V SMD	PC	1,000	D720	.	.	.	.
541	V30007668	IC SDA9400	PC	1,000	IC600	.	.	.	.
542	V30007739	IC LM317T D2PAK	PC	1,000	IC602	.	.	.	.
543	V30007760	DIODE ZENER SMD BZT55C10	PC	1,000	D850	.	.	.	.
544	V30007761	DIODE ZENER SMD BZT55C3V6	PC	1,000	D400	.	.	.	.
545	V30010349	IC DDP3310	PC	1,000	IC601	.	.	.	.
546	V30012506	RES SMD 1/16W 1.5K J (0603)	PC	1,000	R696	.	.	.	.
547	V30012509	RES SMD 1/16W 100K J (0603)	PC	3,000	R913	R914	R786	.	.
548	V30012510	RES SMD 1/16W 100R J (0603)	PC	26,000	R402	R403	R405	R406	R421
.	.	.	.	.	R422	R601	R629	R635	R641
.	.	.	.	.	R689	R690	R691	R692	R693
.	.	.	.	.	R694	R760	R762	R777	R778
.	.	.	.	.	R889	R890	R949	R829	R787
.	.	.	.	.	R835	.	.	.	.
549	V30012559	CAP SMD 10PF 50V D COG (0603)	PC	2,000	C668	C906	.	.	.
550	V30012565	CAP SMD 1.8PF 50V J CH (0603)	PC	2,000	C417	C418	.	.	.
551	V30012568	CAP SMD 270PF 50V J (0603)	PC	9,000	C440	C612	C615	C620	C646
.	.	.	.	.	C650	C655	C656	C746	.
552	V30012569	CAP SMD 33PF 50V J (0603)	PC	6,000	C736	C737	C875	C876	C405
.	.	.	.	.	C404	.	.	.	.
553	V30012570	CAP SMD 330PF 50V J (0603)	PC	7,000	C670	C903	C904	C905	C887
.	.	.	.	.	C889	C891	.	.	.
554	V30012572	CAP SMD 390PF 50V J (0603)	PC	4,000	C679	C682	C693	C441	.
555	V30012573	CAP SMD 47PF 50V J (0603)	PC	1,000	C700	.	.	.	.
556	V30012574	CAP SMD 470PF 50V J (0603)	PC	1,000	C699	.	.	.	.
557	V30012576	CAP SMD 56PF 50V J CH (0603)	PC	2,000	C410	C422	.	.	.
558	V30012577	CAP SMD 560PF 50V J (0603)	PC	8,000	C613	C616	C621	C637	C648
.	.	.	.	.	C651	C654	C657	.	.
559	V30012581	CAP SMD 1NF 50V K R (0603)	PC	14,000	C419	C420	C421	C425	C446
.	.	.	.	.	C447	C457	C458	C465	C466
.	.	.	.	.	C471	C623	C455	C456	.
560	V30012582	CAP SMD 10NF 50V K R (0603)	PC	8,000	C605	C629	C630	C631	C633
.	.	.	.	.	C634	C635	C666	.	.
561	V30012583	CAP SMD 1.5NF 50V K (0603)	PC	5,000	C662	C676	C684	C685	C686
562	V30012585	CAP SMD 2.2NF 50V K R (0603)	PC	8,000	C614	C617	C622	C636	C647
.	.	.	.	.	C652	C653	C658	.	.
563	V30012589	CAP SMD 4.7NF 50V K (0603)	PC	2,000	C461	C462	.	.	.
564	V30012590	CAP SMD 47NF 50V K (0603)	PC	4,000	C661	C677	C681	C691	.
565	V30012608	CAP SMD 27PF 50V J CH (0603)	PC	2,000	C618	C619	.	.	.
566	V30012609	CAP SMD 68NF 50V K (0603)	PC	3,000	C675	C687	C695	.	.
567	V30012613	CAP SMD 3.3PF 50V C CH(0603)	PC	2,000	C601	C602	.	.	.
568	V30012641	RES SMD 1/16W 10K J (0603)	PC	31,000	R400	R401	R622	R652	R654
.	.	.	.	.	R655	R659	R761	R763	R779
.	.	.	.	.	R780	R801	R896	R901	R909
.	.	.	.	.	R929	R683	R917	R816	R822
.	.	.	.	.	R825	R826	R899	R623	R781
.	.	.	.	.	R782	R788	R802	R836	R837
.	.	.	.	.	R830	.	.	.	.
569	V30012650	RES SMD 1/16W 15K J (0603)	PC	5,000	R656	R657	R758	R759	R819
570	V30012657	RES SMD 1/16W 1K J (0603)	PC	31,000	R407	R408	R431	R432	R433
.	.	.	.	.	R434	R439	R606	R634	R640
.	.	.	.	.	R646	R661	R720	R771	R772
.	.	.	.	.	R789	R790	R791	R792	R793
.	.	.	.	.	R797	R807	R919	R920	R626
.	.	.	.	.	R658	R818	R409	R410	R435
.	.	.	.	.	R436	.	.	.	.
571	V30012659	RES SMD 1/16W 2.2K J (0603)	PC	4,000	R651	R764	R765	R840	.
572	V30012661	RES SMD 1/16W 2.4K J (0603)	PC	1,000	R650	.	.	.	.
573	V30012668	RES SMD 1/16W 220R J (0603)	PC	5,000	R605	R633	R639	R645	R795
574	V30012669	RES SMD 1/16W 22K J (0603)	PC	4,000	R625	R721	R918	R647	.
575	V30012673	RES SMD 1/16W 270R J (0603)	PC	1,000	R648	.	.	.	.
576	V30012675	RES SMD 1/16W 2K J (0603)	PC	1,000	R708	.	.	.	.
577	V30012677	RES SMD 1/16W 3.3K J (0603)	PC	2,000	R752	R753	.	.	.
578	V30012679	RES SMD 1/16W 3.9K J (0603)	PC	3,000	R756	R757	R820	.	.
579	V30012688	RES SMD 1/16W 390R J (0603)	PC	4,000	R602	R630	R636	R642	.
580	V30012692	RES SMD 1/16W 4.7K J (0603)	PC	26,000	R404	R417	R418	R419	R420
.	.	.	.	.	R754	R755	R785	R798	R897

BILL OF MATERIAL LIST

10020021 2841 TOSHIBA TOSHIBA 28H37GZ(AK52)

NO	PART NUMBER	DESCRIPTION	UNIT	QTY	POSITION NUMBER				
.	.	.	.	.	R903	R910	R930	R653	R817
.	.	.	.	.	R821	R831	R832	R833	R834
.	.	.	.	.	R902	R663	R823	R824	R838
.	.	.	.	.	R842	.	.	.	.
581	V30012695	RES SMD 1/16W 470R J (0603)	PC	7,000	R895	R900	R908	R928	R898
.	.	.	.	.	R766	R767	.	.	.
582	V30012696	RES SMD 1/16W 47K J (0603)	PC	6,000	R773	R774	R775	R776	R827
.	.	.	.	.	R828	.	.	.	.
583	V30012713	RES SMD 1/16W 75R J (0603)	PC	30,000	R620	R621	R624	R632	R638
.	.	.	.	.	R644	R688	R699	R860	R885
.	.	.	.	.	R886	R904	R906	R911	R931
.	.	.	.	.	R942	R943	R944	R945	R946
.	.	.	.	.	R947	R948	R932	R933	R934
.	.	.	.	.	R935	R936	R937	R905	R951
584	V30012719	RES SMD 1/16W 910R J (0603)	PC	1,000	R697	.	.	.	.
585	V30012982	RES SMD 1/16W 10R J 0603	PC	12,000	R603	R631	R637	R643	R662
.	.	.	.	.	R892	R907	R921	R927	R894
.	.	.	.	.	R649	R893	.	.	.
587	V30013001	RES SMD 1/16W 1K F (0603)	PC	1,000	R841	.	.	.	.
588	V30013571	IC SDA5550	PC	1,000	IC722	.	.	.	.
589	V30013686	IC VIDEO SWITCH TEA6415CDT SMD	PC	1,000	IC851	.	.	.	.
590	V30014022	RES SMD 1/16W 47R J (0603)	PC	2,000	R794	R796	.	.	.
591	V30014128	RES SMD 1/16W 33R J (0603)	PC	2,000	R604	R938	.	.	.
592	V30015059	IC VPC3230D	PC	1,000	IC603	.	.	.	.
593	V30016126	CAP SMD 220NF 16V K R (0603)	PC	1,000	C842	.	.	.	.
594	V30016654	CAP SMD 100NF 16V K R (0603)	PC	43,000	C411	C423	C424	C449	C600
.	.	.	.	.	C607	C608	C609	C610	C611
.	.	.	.	.	C625	C626	C632	C664	C672
.	.	.	.	.	C673	C678	C692	C720	C724
.	.	.	.	.	C727	C728	C730	C732	C733
.	.	.	.	.	C734	C739	C740	C741	C742
.	.	.	.	.	C744	C745	C750	C883	C885
.	.	.	.	.	C886	C893	C895	C897	C898
.	.	.	.	.	C752	C400	C884	.	.
595	V30017143	COIL SMD 22UH (2520)	PC	14,000	L402	L403	L404	L405	L412
.	.	.	.	.	L413	L416	L417	L600	L720
.	.	.	.	.	L724	L862	L414	L415	.
596	V30018093	COIL SMD 3.3uH (2520)	PC	13,000	L726	L857	L858	L859	L854
.	.	.	.	.	L855	L856	L851	L852	L853
.	.	.	.	.	L723	L721	L722	.	.
597	V30018409	RES SNETWORK 1/16W 330R J (0603)	PC	15,000	R700	R701	R702	R703	R704
.	.	.	.	.	R705	R706	R707	R808	R809
.	.	.	.	.	R810	R811	R812	R813	R814
598	V30020535	DIODE ZENER SMD BZT55C3V9	PC	1,000	D751	.	.	.	.
599	V20128394	MD.SMD.FB52A3-FASTEXT	PC	1,000	.	.	.	.	.
600	V30012580	CAP SMD 820PF 50V J (0603)	PC	1,000	C749	.	.	.	.
603	V30001833	CONN HEADER 2P 2.5MM SIDE BLUE SD	PC	1,000	PL855	.	.	.	.
604	V30001844	CONN HEADER 3P 2.5MM SIDE GREEN SD	PC	1,000	PL400	.	.	.	.
606	V30001756	XTAL 18.432MHZ	PC	1,000	X400	.	.	.	.
607	V30001834	CONN HEADER 2P 2.5MM SIDE RED SD	PC	1,000	PL722	.	.	.	.
608	V30001853	SOCKET IC 32P	PC	1,000	IC721	.	.	.	.
609	V30006662	XTAL 6MHZ	PC	1,000	X720	.	.	.	.
610	V30006712	FERRITE BEAD 3.5X4.7X0.8	PC	1,000	L601	.	.	.	.
611	V30007745	CONN HEADER 10P 2.54MM SIDE WHT DR	PC	1,000	PL853	.	.	.	.
612	V30008778	XTAL 20.25MHZ	PC	1,000	X600	.	.	.	.
613	V30008782	XTAL 5MHZ	PC	1,000	X601	.	.	.	.
614	V30009784	SOCKET IC 8P (DIP)	PC	1,000	IC720	.	.	.	.
615	V30018115	CONN HEADER 3P 2.5MM SIDE BD SR	PC	1,000	PL723	.	.	.	.
616	V30018117	CONN HEADER 6P 2.5MM SIDE BD	PC	1,000	PL721	.	.	.	.
617	V30018410	CONN HEADER 35P 3.0MM SIDE DR	PC	2,000	PL857	PL858	.	.	.
619	V30001841	CONN HEADER 3P 2.5MM SIDE BLACK SD	PC	1,000	PL401	.	.	.	.
621	V20131458	PR.IC.52-AK52B-FASTEXT TOSHIBA T022	PC	1,000	.	.	.	.	.
622	V30018652	IC SST37VF040 4MBIT 3.3V PDIP-32	PC	1,000	IC721	.	.	.	.
623	V30009846	CABL 1P/40 SIS	PC	1,000	KX20	.	.	.	.
624	V20124498	IC 24C32 A059311112111221211	PC	1,000	.	.	.	.	.
625	V30015382	IC 24C32 3V	PC	1,000	.	.	.	.	.
626	V20130616	CRT DIFF.KIT AK52B-28" 4:3 VCL 135V(TOSH	PC	1,000	.	.	.	.	.
627	V30000094	CAP MKT 220NF 275V M AC	PC	1,000	C802	.	.	.	.
628	V30000121	CAP KP 27NF 630V J	PC	1,000	C111	.	.	.	.
629	V30000167	CAP MKP 560NF 250V J	PC	1,000	C112	.	.	.	.
630	V30000177	CAP MKP 820NF 250V J	PC	1,000	C114	.	.	.	.
631	V30000179	CAP MKP 9.1NF 1600V %3.5	PC	1,000	C110	.	.	.	.
632	V30001110	RES MO 1W 1.5R J	PC	1,000	R139	.	.	.	.
633	V30001124	RES MO 3W 220R J	PC	1,000	R140	.	.	.	.
634	V30001174	RES MO 2W 0.47R J	PC	1,000	R141	.	.	.	.
635	V30001217	RES FUSE 2W 1.2R J	PC	1,000	R128	.	.	.	.
636	V30001244	RES FUSE 1/2W 0.47R J	PC	1,000	R124	.	.	.	.
637	V30001246	RES FUSE 1W 0.47R J	PC	1,000	R130	.	.	.	.
639	V30007756	COIL BRIDGE 150UH 32KHZ AK28	PC	1,000	L104	.	.	.	.
640	V30010517	CAP MKT 33NF 100V K	PC	1,000	C102	.	.	.	.
641	V30014943	CAP MKP 3.9NF 1600V J	PC	1,000	C109	.	.	.	.
642	V30017521	TRF FBT SINGLE COMMON FOCUS LAYER (AK41)	PC	1,000	TR101	.	.	.	.
643	V30018304	LINEARTY COIL 7UH	PC	1,000	L103	.	.	.	.
644	V30018581	RES MO 2W 150R J	PC	1,000	R101	.	.	.	.
645	V20124500	SCR.AS.2841 W/SB (AK52)(V0)	PC	1,000	.	.	.	.	.
646	V20120113	BACK DOOR AK45/52 (I) (V.0)	PC	1,000	.	.	.	.	.
647	V60000009	FR-HIPS NATR.V-0	KG	0,060	.	.	.	.	.
648	V60000022	MASTERBATCH (BLACK)	KG	0,006	.	.	.	.	.
649	V35000211	SCREW S C ZNSY YSMB 2.9*9.5	PC	4,000	.	.	.	.	.
650	V35000212	SCREW S C ZNSY YSMB 2.9*13	PC	2,000	.	.	.	.	.
651	V35000224	SCREW C SK ZN YFMB 2.9*9.5	PC	16,000	.	.	.	.	.
652	V35000231	SCREW SK C NI YFMB 2.9*6.5	PC	5,000	.	.	.	.	.
653	V35004572	SCREW P C AgSYF YSB 4x20	PC	10,000	.	.	.	.	.
654	V35006331	SCREW P C ZN AKBR 7*26	PC	4,000	.	.	.	.	.
655	V40000082	FOOT RUBBER 8410/11	PC	2,000	.	.	.	.	.

BILL OF MATERIAL LIST

10020021 2841 TOSHIBA TOSHIBA 28H37GZ(AK52)

NO	PART NUMBER	DESCRIPTION	UNIT	QTY	POSITION NUMBER				
656	V20124506	BACK CVR.2841/42/44 W/SB(UL)MATBLK(P)4:3	PC	1,000	.	.	.	.	.
657	V20124505	BACK C.2841/42/44 W/SB(UL)(I)(BOYAN.)4:3	PC	1,000	.	.	.	.	.
658	V60000009	FR-HIPS NATR.V-0	KG	2,413	.	.	.	.	.
659	V60000022	MASTERBATCH (BLACK)	KG	0,012	.	.	.	.	.
660	V60000950	PAINT AKAI FUME-022-4929(SU BAZ)L8341321	KG	0,080	.	.	.	.	.
661	V20124820	MD.ASY.SB103-FAV+HP+SVHS XX41/W (AK52)	PC	1,000	.	.	.	.	.
664	V30001830	CONN HEADER 2P 2.5MM TOP BLUE SD	PC	1,000	PL106	.	.	.	.
665	V30001839	CONN HEADER 3P 2.5MM TOP GREEN SD	PC	1,000	PL107	.	.	.	.
666	V30001891	RCA JACK 1P WHITE 28 FAV	PC	1,000	JK102	.	.	.	.
667	V30001892	RCA JACK 1P RED 28 FAV	PC	1,000	JK103	.	.	.	.
668	V30001893	RCA JACK 1P YELLOW 28 FAV	PC	1,000	JK101	.	.	.	.
670	V30001838	CONN HEADER 3P 2.5MM TOP YELLOW SD	PC	1,000	PL105	.	.	.	.
671	V30001895	JACK 4P DIN TYPE FOR SVHS	PC	1,000	JK105	.	.	.	.
673	V30001902	JACK HEADPHONE STEREO WO/SW	PC	1,000	JK108	.	.	.	.
674	V30020932	CNAS 3P/550 FLT W/BLK C+FER UL2468AWG24	PC	1,000	PL108	.	.	.	.
676	V30020137	CNAS 600 FAV SVHS W/DC+FER	PC	1,000	PL106	.	.	.	.
683	V30000594	RES CF 1/4W 22K J	PC	2,000	R102	R104	.	.	.
684	V30000712	RES CF 1/4W 470R J	PC	2,000	R103	R106	.	.	.
685	V30001979	FIXED COIL 1UH Q45 M-A	PC	1,000	L101	.	.	.	.
686	V30019363	PCB 11SB103-2	PC	1,000	.	.	.	.	.
687	V30000190	CAP CER 100PF 50V J CH	PC	3,000	C101	C103	C104	.	.
693	V30000650	RES CF 1/4W 33R J	PC	2,000	R110	R111	.	.	.
694	V30001979	FIXED COIL 1UH Q45 M-A	PC	1,000	L102	.	.	.	.
695	V30000190	CAP CER 100PF 50V J CH	PC	1,000	C102	.	.	.	.
699	V30000115	CAP MKT 6.8NF 100V J	PC	2,000	C105	C106	.	.	.
701	V30006712	FERRITE BEAD 3.5X4.7X0.8	PC	1,000	FXX1	.	.	.	.
702	V20125820	ARTWORK TOSH.TOSHIBA 28H37GZ(AK52)	PC	1,000	.	.	.	.	.
703	V20124499	R/C 2143 TOSHIBA CT-841 (GRAY/S)	PC	1,000	.	.	.	.	.
704	V20095313	R/C 2143 NOBRAND (F)	PC	1,000	.	.	.	.	.
705	V20094768	R/C KIT 2143 TOSHIBA	PC	1,000	.	.	.	.	.
706	V20094767	MD.ASY.UK05	PC	1,000	.	.	.	.	.
707	V20094766	UKV.B.ASSY.UK05 (SMD)	PC	1,000	.	.	.	.	.
708	V30000489	RES SMD 1/10W 1R J (0805)	PC	1,000	R102	.	.	.	.
709	V30012509	RES SMD 1/16W 100K J (0603)	PC	1,000	R103	.	.	.	.
710	V30012510	RES SMD 1/16W 100R J (0603)	PC	1,000	R100	.	.	.	.
711	V30012578	CAP SMD 68PF 50V J (0603)	PC	2,000	C101	C102	.	.	.
712	V30016654	CAP SMD 100NF 16V K R (0603)	PC	2,000	C103	C104	.	.	.
713	V30018063	IC HT48RA0A OTP	PC	1,000	IC101	.	.	.	.
714	V30018712	PCB 11UK05-2	PC	1,000	.	.	.	.	.
715	V30000352	CAP EL 100UF 16V M	PC	1,000	C100	.	.	.	.
716	V30001453	TR BC337	PC	1,000	Q100	.	.	.	.
717	V30002733	LED INFRARED IR333	PC	1,000	D100	.	.	.	.
718	V30002852	XTAL REZ 455KHZ	PC	1,000	X100	.	.	.	.
719	V35002401	BATTERY CONT.SINGLE (-) RC2040	PC	1,000	.	.	.	.	.
720	V35005008	BATTERY CONT.SINGLE (+) RC2040 TOSHIBA	PC	1,000	.	.	.	.	.
721	V35000228	SCREW SK C ZNSY YSMB 2.9*9.5	PC	1,000	.	.	.	.	.
722	V35005007	DOUBLE BATTERY CONTACT UKV-900 TOSHIBA	PC	1,000	.	.	.	.	.
723	V40005467	LENS RC2040(I)	PC	1,000	.	.	.	.	.
724	V40010082	RUBBER PAD TRP41 (RC 2143) TOSHIBA	PC	1,000	.	.	.	.	.
725	V40012344	SPONGE (BATTERY DOOR) (15x31x5mm)	PC	1,000	.	.	.	.	.
726	V40005213	BATTERY COVER RC2040(I)	PC	1,000	.	.	.	.	.
727	V40007377	BOTTOM CVR R/C 21/2240 (I)	PC	1,000	.	.	.	.	.
728	V40010356	TOP CVR R/C 2143 NOBRAND (S)	PC	1,000	.	.	.	.	.
729	V30002391	BATTERY AAA UM4 1.5V GREEN	PC	2,000	.	.	.	.	.
730	V50038144	I/B TOSHIBA 28H37GZ P/92195/2143/GESIPFD	PC	1,000	.	.	.	.	.
731	V20125882	LBL.BCK.CVR.TOSHIBA TOSHIBA 28H37GZ "52"	PC	1,000	.	.	.	.	.
732	V20013018	LBL.BCK.CVR.ASSY (TV) (WO/UL)	PC	1,000	.	.	.	.	.
733	V50023173	LABEL LOT W/BARCODE (77X256)	PC	1,050	.	.	.	.	.
734	V70000621	RIBBON 80MM*450MM	PC	1,030	.	.	.	.	.
735	V20125883	LBL.CART.BOX TOSHIBA 28H37GZ(ÇÝFT KATLI)	PC	1,000	.	.	.	.	.
736	V50023532	LABEL LOT TOSHIBA ÇÝFT KATLI	PC	1,050	.	.	.	.	.
737	V70000621	RIBBON 80MM*450MM	PC	1,050	.	.	.	.	.
738	V30002754	28" CPT TUBE 100 HZ FLAT IRON	PC	1,000	.	.	.	.	.
739	V40009510	LOGO TOSHIBA (W/P-SILVER BRUSH/H.ST)	PC	1,000	.	.	.	.	.
740	V50000007	PLASTIZOTE (1400*1000)	PC	1,000	.	.	.	.	.
741	V50031267	LABEL EHT/27.8KV BEAM/1050uA (GER)	PC	1,000	.	.	.	.	.

Cabinet Exploded View

N/A

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